

Metal-Organic Framework nano-layers for capacitive gas sensing

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Summary:

In this project, novel metal-organic frameworks (MOFs) will be evaluated for the implementation into gas sensing devices. MOFs are molecular sieves with pores in the nm-range. A MOF layer with a thickness of several nanometres shall be coated on a Si-based capacitor. If molecules from a gas mixture enter selectively the MOF layer, the capacity of the capacitor will change in a characteristic way. There are two main routes for selective gas sensing using (i) the molecular sieve effect, which means that only molecules smaller than the pores can become adsorbed, or (ii) strong adsorption on specific sorption sites like accessible metal ions in the walls of the MOF structure.

The synthesis of MOFs as thin films allows their integration into different electronic devices. Particularly, their application in metal-insulating-semiconductor (MIS) capacitors requires a comprehensive study of the electric transport mechanism. Only a low concentration of border traps guarantees a good performance of MIS capacitors.

By a newly developed spraying technique, 5 nm thin MOF layers of the structure type Cu₃BTC₂ (also named HKUST-1) have been sprayed onto p-Si wafers to be incorporated in metal-insulator-semiconductor (MIS) capacitors. In this MOF, Cu²⁺ ions are bridged by benzene-1,3,5-tricarboxylic acid as linker. In this 0.9 nm wide pore structure, the copper sites are accessible for gas molecules and specific adsorption of olefins, ammonia, nitrogen oxides to the copper sites can be expected.

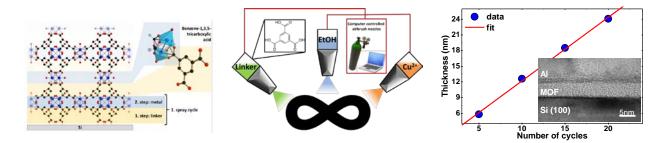


Figure 1: MOF structure, spraying principle and sprayed thin-layer MOF. film.

(a) Porous structure of HKUST-1, epitaxial grown on Si by spraying cycles (1st and 2nd cycle are indicated). Pore size about 0.9 nm. (b) Principle of the formation of MOF layers by spraying. Alternating, linker solution, washing by ethanol, metal solution, washing by ethanol, linker solution... are sprayed. So layer-by-layer, the MOF structure is formed. (c) Transmission electron microscopy of the 5 nm thick MOF layer of HKUST-1 on p-Si. Note that there is a perfect correlation between the number of spraying cycles and the thickness of the MOF layer. On top of the MOF layer are Al contacts as sketched in Figure 2. Boron-doped p-type silicon (p-Si) wafers with (100)-orientation, 525 μ m thickness and 0.5-0.75 Ω cm resistivity were used for device fabrication. First, aluminium was evaporated as the back electrode and annealed in forming gas in order to form a good Ohmic contact. Second, thin Cu₃(BTC)₂ films were synthesized by the spray-coating method in a layer-by-layer growth mode. Different layer thicknesses were achieved by increasing the number of spray cycles. Finally, circular Al electrodes were deposited topside using a shadow mask. Figure 2 shows the device structure and the occupancy of the oxide charges inside the p-Si/Cu₃(BTC)₂/Al MIS capacitor.

Before we can start with gas sensing, the charge traps in such MIS device must be characterized since such trapped electric charges can influence or even spoil the performance of the sensor. Fixed charges are located in the dielectric layer. These fixed charges cannot communicate with the substrate. Interface charge traps are located at the MOF/Si interface. Border electric charge traps are located close to – but not at – the MOF/Si interface. In contrast to fixed charges, the interface and border traps can be charged during the voltage sweep and therefore they can exchange charges with the Si conduction band, however, with different time responses. The electrical characterization was performed via capacitance-voltage (C-V) measurements in forward and reverse direction at room temperature at different frequencies. Figure 2(b) shows the total border trap density for different gate voltage for two frequencies.

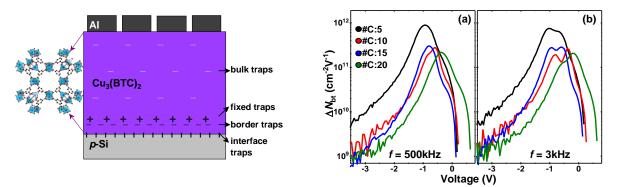


Figure 2: Device and electric border trap densities from C-V measurements.

(a) Device structure of the p-Si/Cu₃(BTC)₂/AI MIS capacitor showing the location of the different charges which can be present in the device.

(b) Total border trap density as a function of the applied gate voltage of the p-Si/Cu₃(BTC)₂/AI MIS capacitor measured at 500 kHz (a) and at 3 kHz # indicates the number of spray cycles (MOF unit cells in the layer) as shown in Figure 1 (c).

In conclusion, the formation of hysteresis in the bidirectional capacitance measurements suggests the existence of border traps. Charge transport occurs in two sequential steps: (i) Injection of electrons from the gate to the traps close to the Al/Cu₃BTC₂ interface, and (ii) transport towards the border traps located close to the Cu₃BTC₂/Si interface. Low border trap density values between 10¹¹-10¹² cm⁻²eV⁻¹ were extracted from the hysteretic behaviour signifying low electron trapping processes. The low fixed positive charges and the relatively low concentrations of border traps in the Cu₃(BTC)₂ recommend the use of this MOF as a dielectric layer in capacitor-based sensors. The density of border traps can be most likely further reduced by annealing.

Meanwhile the spraying apparatus has been transferred from Physical Chemistry to the Institute of Electronic Materials and Devices to continue the coatings.

For more details see L. Montanez, I. Strauß, J. Caro, H.J. Osten, Impact of border traps in ultrathin metal-organic framework Cu₃(BTC)₂ based capacitors, Microporous Mesoporous Materials 277 (2018) 136-141.