RESEARCH FORUM 2004

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Never stop thinking.

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Welcome to the Infineon Research Forum 2004

The just started transition from microelectronics to nanoelectronics with sub 100nm structure has opened up another round of enormous potential for semiconductor applications. The increasing production and use of semiconductor devices is also demanding new concepts and methods, how to run and link this devices efficiently by using advanced systems and concepts. Corporate Research is focused therefore in particular to ensure the continuity of Moore's Law, but also to increase the efficiency of the devices by advanced system and architecture solutions. Furthermore, we are already looking in new solutions and options beyond the current state-of-the-art.

Corporate Research is structured in seven competence centers (Nano Processes, Nano Devices, Advanced Mixed Signal Applications, High Frequency Circuits, Photonics, Systems Technology and Emerging Technologies). The groups work closely together to enable future semiconductor applications and also to propose new fields of application.

A quick journey through the topics covered at Corporate Research start at the heart of semiconductors at the transistor. We are working on concepts to shrink CMOS transistors below 20nm with ultra-short gates and ultra-thin channels. We are using new methods and materials like SOI and carbon nanotubes to achieve such small feature. This combination of top down features size reduction and the combination of bottom-up grown nano structures (e.g. nanotubes) is one possible path to extend Moore's Law to features below 10nm. Furthermore, we are also investigating multi-gate devices and new non-volatile memory concepts. We have shown that double gates can help to improve the scalability. Another topic of major interest are future interconnect solutions. We are investigating the scaling behaviour of Al and Cu and are also looking in new carbon based materials. Beside new transistor and interconnect concepts, CPR is also delivering the methods to manufacture this new devices. Additionally we are also investigation the interface between semiconductor devices and biological cells to allow new applications. Based on the devices we are looking into methods and circuit designs to allow high frequency applications based on CMOS and SiGe, which are targeted for applications in the filed of automotive and communication. For high speed data communication we are developing novel laser modulators. Further work is targeted to develop new system concepts and applications to drive the integration of multiple devices and to improve the interfaces to the user. Examples are innovative cell phone architectures and advanced man-machine communication systems. Finally, we are also working on emerging technologies such as wearable electronics and ambient intelligence systems. The quick journey through our work reveals that Corporate Research is able to address all major technological challenges on the path form the single transistor to the fully integrated system.

The groups of Corporate Research have received outstanding results during the last month, which had been attracting high awareness not only at our customers but also in the press and media. Based on these great results, CPR runs joint projects with all business groups within Infineon and external partners. New applications are also deployed together with our Infineon Venture Group. Our experts are involved in cross functional projects and are ready to work with our customers on new solutions. CPR has a clear focus to be a first class partner in our cooperations. We want to use the opportunity to thank our partners, customers and the authorities for their great support.

Also in the future CPR will work with partners and customers on new solutions, to support Infineon on its way to become the leading semiconductor company, enabling the lifestyle of the 21st century.

The Infineon Research Forum is a key platform to drive the dialogue between researchers and customers, to accelerate transfers from research to business and to exchange on new applications. CPR is looking forward to a fruitful dialog with our customers and partners.

Your CPR Team

Nano Processes

Introduction

Our objective is to prove the functionality of devices in the nanometer regime long before going into production, detecting roadblocks and bottlenecks. We apply appropriate processes, sometimes not those that will eventually be used in production in ten years, but which are available now. Our facility consists of three class 10-1000 cleanrooms that house the equipment necessary for key processes and analytics. Wafers can be handled and controlled in a qualified way so that transfer to and from production lines for standard processing is possible. Most of the equipment is capable of processing 6 & 8” wafers and 300 mm will soon come. For very advanced processing with new materials we provide a separate cleanroom area to avoid interference with contamination-free wafers. Cleanroom infrastructure is supported by each member of the technology groups ND, NP and PH, hence no dedicated personal is allocated.

Dr. Wolfgang Hönlein
Phone +49 (0)89 234-44397
E-mail wolfgang.hoenlein@infineon.com

Nanointerconnects

How do interconnects behave in the nanometer regime?

Modern VLSI chips comprise of up to more than 10 levels of metallic interconnects that are needed for the transport of signals. The lengths range from very short lines for local connections to lines of the order of the chip dimensions (cm) for bus, clock and power supply systems. Lower levels close to the densely packed active device (transistor) layer have to be fabricated in the smallest widths available. Thus, local lines follow the scaling of the transistors.

Once the width of a metal line or the size of its grains reaches the mean free path of the electrons in that material, the transport process can no longer be treated as for a bulk metal. Additional scattering at the boundaries of the line and at the grain boundaries has to be taken into account (Fig. 1). The resistivity will increase as the line width shrinks below values of approx. 100 nm. We have investigated line widths in the range of 20 nm to 300 nm for different interconnect metals. Fig. 2 shows, that the

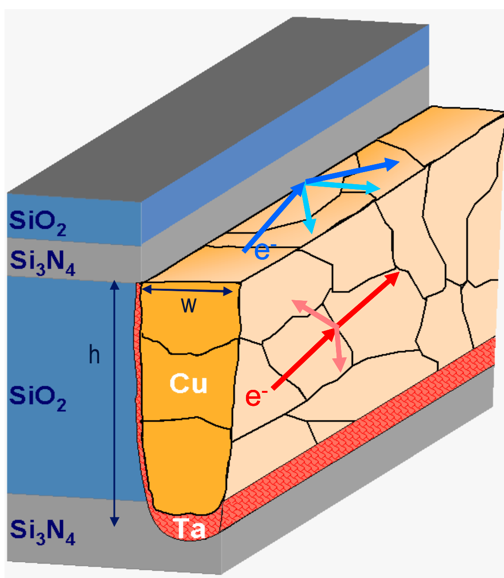


Figure 1: Additional scattering at grain boundaries and at the surface has to be taken into account for narrow wires.

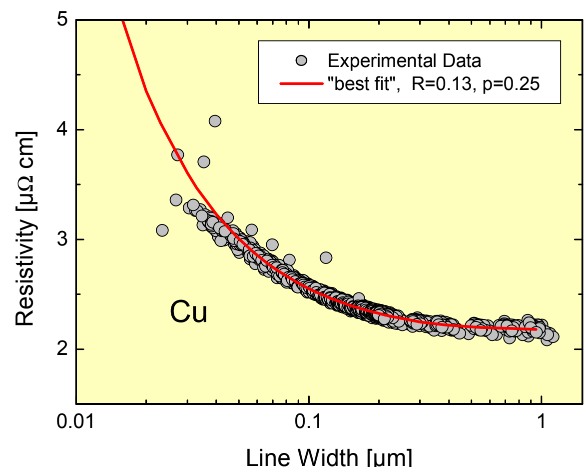


Figure 2: The size effect leads to an increase in resistivity as a function of line width. The results can be fitted very well by a combined surface and grain boundary scattering model.

resistivity increases considerably from the bulk value for smaller line widths, independent of the material.

As a result, signal propagation will be delayed, counteracting the increase in switching speed that can be realized with smaller transistors. We have developed a model that takes into account additional scattering by the conductor interface and the grain boundaries.

Fig. 3 shows good agreement between experimental data and theory for a wide range of temperatures. It can also be seen from Fig. 3 that cooling lowers the resistivity but size effects are independent of the temperature and cannot be reduced.

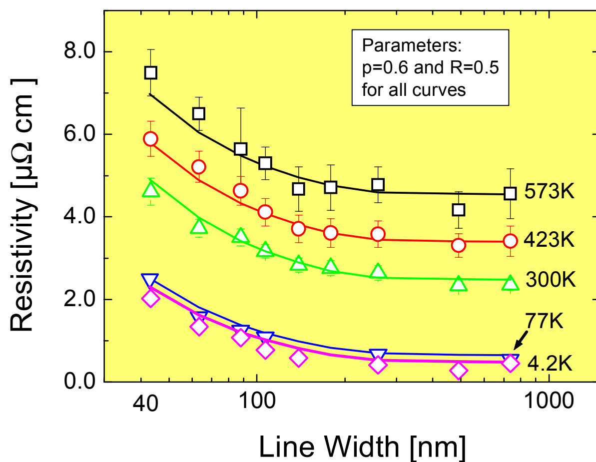


Figure 3: *Temperature dependence of the size effect. Cooling lowers the resistivity but the additional scattering is independent of temperature.*

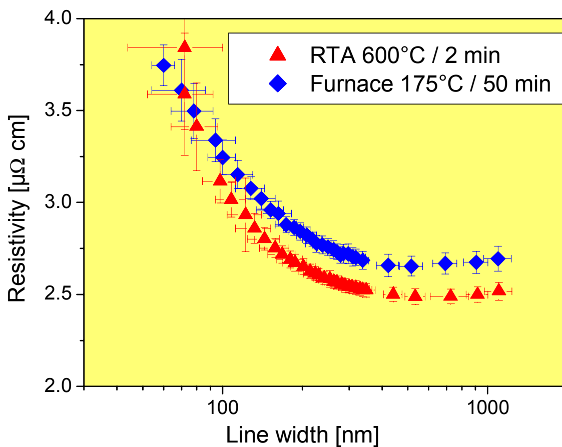


Figure 4: *Thermal treatment influences the grain sizes, but at small line widths the difference vanishes.*

According to our model we expect reduced resistivity degradation if the medium grain size can be increased. In Fig. 4 we have treated metal lines with different thermal annealing processes, showing a lower resistivity for larger grain sizes. However, as line width decreases, differences in resistivity diminish and vanish completely for the smallest line widths. Obviously, the grain size adjusts to the line dimensions. It is one of our technological goals for the future to find a method to increase the medium grain size beyond the dimensions of the line cross-section.

The scaling of copper diffusion barriers

The material of choice for interconnects is copper. On the other hand copper has detrimental effects on the properties of the semiconductor, and one has to take care that copper does not diffuse to the silicon interface. It is, therefore, mandatory to have a diffusion barrier encapsulating the copper lines (Fig. 5). Common barrier materials are tantalum nitride/tantalum or titanium/titanium nitride. The resistivity of these material combinations is roughly a factor of ten worse than copper. The standard barrier layer is already as thin as 28 nm and further reduction might eventually be detrimental to the prevention of copper diffusion. Further, if a certain barrier thickness is mandatory, the resistivity degradation with line width would be accelerated because of the reduction of the copper cross-section.

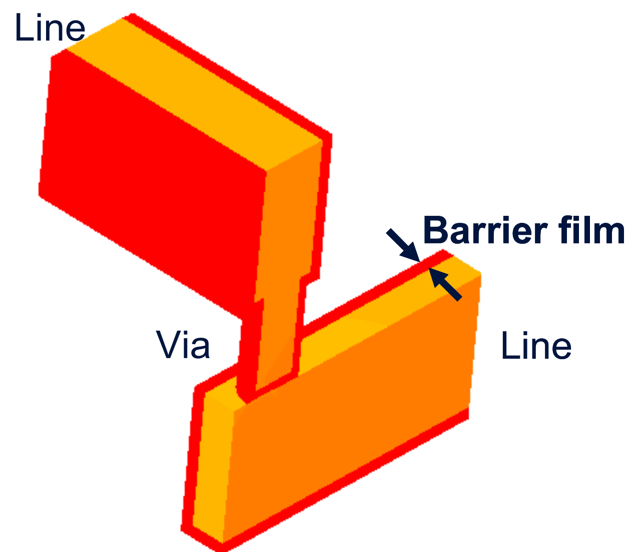


Figure 5: *Barrier layers (red) encapsulate the copper lines and vias (yellow) to prevent the detrimental diffusion of copper.*

We have, therefore, investigated the barrier integrity as a function of barrier thickness. As an indicator of barrier integrity we have measured the leakage current between two adjacent long metal lines. The increase of the electrical field yielded the breakdown behaviour as shown in Fig. 6.

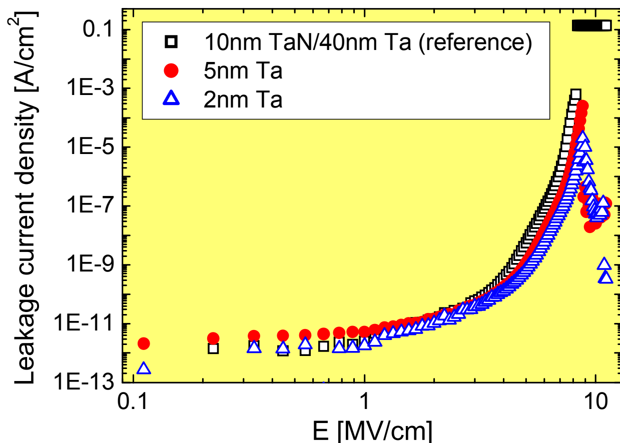


Figure 6: *Electrical breakdown of two adjacent metal lines for different barrier thicknesses.*

Reducing the barrier thickness to values close to 1 nm did not result in a measurable increase of the leakage current. Even annealing at temperatures far above the normal operating conditions (450°C), did not increase the leakage. The scaling of diffusion barriers will, thus, not be a roadblock for the prevention of copper diffusion on our way to nanometer dimensions.

Reduction of parasitic capacitances

Narrow conductor lines, especially those for global interconnects, suffer from crosstalk due to increased parasitic capacitance. A common way of reducing capacitance is to introduce new dielectric materials with lower permittivity into the process flow. A drawback of this approach is the introduction of new and technologically risky materials, that might cause reliability and yield problems when combined with the silicon technology. In addition, low-k concepts often lead to only minor changes in the effective reduction of the permittivity, because additional auxiliary layers with higher k have to be introduced.
At CPR NP we have developed a method to create voids in a defined way between the narrow metal lines, the so-called air-gaps (Fig. 7).
The absence of dielectrics would bring the k-value down to the lowest possible value of 1.

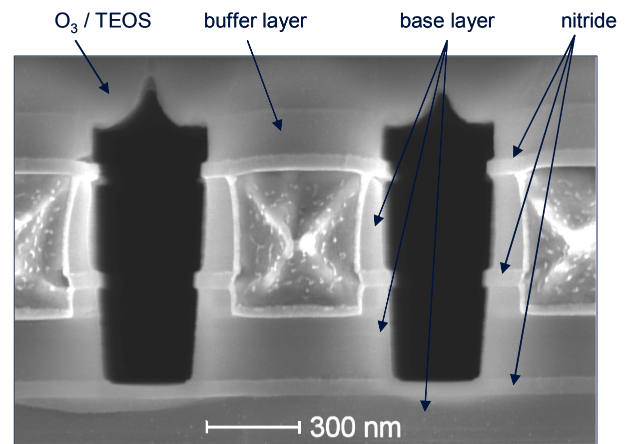


Figure 7: *SEM cross-section of an airgap structure. Metal lines are separated by deliberately created voids.*

However, the auxiliary layers that are still needed to support the metal structure, spoil this theoretical limit. By using extensive simulations we were able to optimize the air-gap structure so that subsequent experiments achieved values as low as k=2.5 using only conventional materials (Fig. 8).

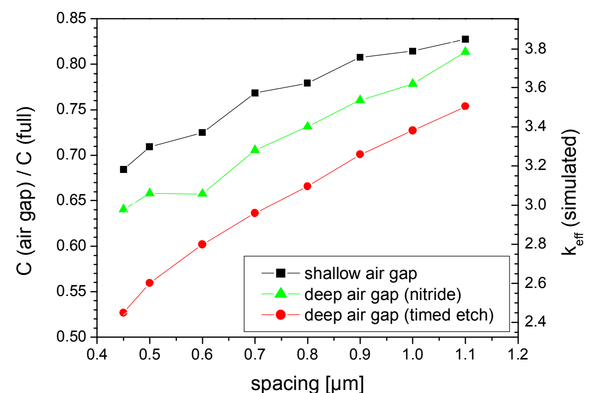


Figure 8: *Experimental values for the reduction in parasitic capacitance between two neighbouring copper lines for different airgap geometries as a function of line spacing. The red line shows that for the geometry shown in Fig. 7 the line-to-line capacitance is reduced by nearly a factor of 2.*

It should be noted that, for the time being, the introduction of air-gaps is at the expense of an additional mask. However, the mask can be used to place the air-gaps specifically at sites that are prone to crosstalk, thus minimizing the risk of reliability problems. We are currently also investigating a maskless, self-aligned solution.

How else can we manage signal delay?

Technological solutions for scaling problems have been readily available in the past to circumvent obstacles in the further miniaturization of silicon devices. However, the introduction of new and exotic materials and concepts will impose additional risks and costs on the silicon technology. Consequently, the trade-off between technological and design solutions will increase. Even including the size effects discussed above, a metal line will still have a resistance that is two orders of magnitude lower than a semiconducting transistor. As a consequence, for local wires up to approx. 100F (F=minimum lithographic length) the transistor governs the delay of the total system (transistor + wire). If designers are aware of this they can take it into account, e.g. by keeping the narrow wires shorter and using hierarchical wiring with broad wires in the upper layers. One of our conclusions for the future is, therefore, that the optimization of the total system can only be achieved by a closer and earlier collaboration between technologists, designers and system architects.

New technological approaches: Crystalline wires

We have shown in the previous chapter that a reduction in resistivity only can be achieved by eliminating the scattering centers in the metals. It is clear that monocrystalline wires would be ideal for that application. In the following section we present results from a totally different approach, namely the incorporation of nanotechnology methods to build crystalline wires and even transistor structures.

Dr. Manfred Engelhardt,
Phone +49 (0)89 234-55321
E-mail manfred.engelhardt@infineon.com

Dr. Günther Schindler
Phone +49 (0) 89 234-50832
E-mail guenther.schindler@infineon.com

Dr. Werner Steinhögl
Phone +49 (0)89 234-44679
E-mail werner.steinhoegl@infineon.com

Dr. Gernot Steinlesberger,
Phone +49 (0)89 234-49748
E-mail gernot.steinlesberger@infineon.com

Dr. Martin Traving
Phone +49 (0)89 234-55207
E-mail martin.traving@infineon.com

Dr. Werner Pamler
Phone +49 (0)89 234-49662
E-mail werner.pamler@infineon.com

Zvonimir Gabric,
Phone +49 (0)89 234-48128
E-mail zvonimir.gabric@infineon.com

Carbon Nanotubes for Microelectronics

Carbon nanotubes are a new modification of graphitic carbon, discovered in 1991. They can be thought of as a rolled up piece of a graphite monolayer that forms a seamless cylinder (Fig. 9).

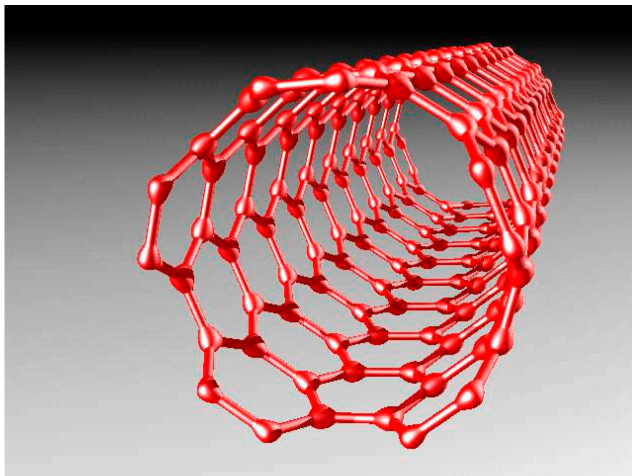


Figure 9: *Carbon nanotubes are graphite monolayers rolled up into seamless cylinders.*

There are different ways of rolling up the layer and each modification turns out to behave differently with respect to electrical conductivity: Two out of three configurations are semiconducting, whereas one third is metallic. The band gap of semiconducting tubes can be tuned by their diameter. As a rule of thumb, nanotubes with 1 nm diameter exhibit energy gaps of approx. 0.8 eV, close to the value of silicon (1.12 eV). Given that the morphology can be controlled, one can tailor the energy gap of the semiconducting tubes. For both modifications there is another striking feature: electron transport is free of scattering because of the one-dimensional nature and the crystalline perfection of the tubes. For the metallic nanotubes this means unsurpassed current densities of up to 10^{10} A/cm², which is about

1000 times that of a bulk metal. Tab. 1 summarizes the most important features for applications in microelectronics.

Table 1: The most important characteristics of carbon nanotubes for applications in microelectronics.

Electrical conductivity	Metallic or semiconducting
Energy gap	E_g [eV] 1/d [nm]
Electrical transport	Ballistic, no scattering
Maximum current density	10^{10} A/cm²
Diameter	1-100 nm
Length	Up to mm
Thermal conductivity	6000 W/(Km)
Maximum strain	0.11% @ 1V

Carbon nanotube growth

Carbon nanotubes can be produced using very different procedures:

1. Ex-situ growth
Nanotubes can be found in the residues of an arc discharge between two graphite rods. Alternatively, nanotubes are produced when a laser hits a graphite target at very high temperatures in a furnace. In both cases nanotubes have to be collected together with other residues. After intensive cleaning procedures nanotubes can be dispersed in a suitable solvent. If the solution is spun onto a wafer with prefabricated contacts, after evaporation of the solvent some tubes may lie between electrical contacts and can be exploited for measurements. As this procedure is not very reproducible and has a low yield we have decided to adopt, and further develop, another procedure that is basically a CVD-process.

***Figure 10:** Infineon logo composed of millions of vertically grown entangled nanotubes on top of a catalyst layer (not visible) that was patterned by lithography.*

2. Catalyst mediated chemical vapor deposition (CCVD)
A carbon containing feedstock gas (e.g. acetylene) is brought into contact with a very thin catalyst layer (e.g. iron) deposited on a substrate. If the layer exhibits the right morphology carbon nanotubes can be grown at the catalyst sites. This method fits better into the silicon process landscape, because growth only occurs where the catalyst is deposited and patterning of the catalyst layer by lithography may help to define the growth sites. In Fig. 10 we show how such a process can be used to build the Infineon logo out of millions of entangled nanotubes.

Carbon nanotubes for interconnects

Carbon nanotubes may also consist of many concentric shells each shell with an individual crystalline configuration. Electron transport is unperturbed in every single shell and metallic shells are always present. These multi-walled carbon nanotubes may, thus, be exploited for conductors. Catalyst mediated CVD, as described in the previous chapter, is ideally suited to grow nanotubes as vertical interconnects between two metal layers. These

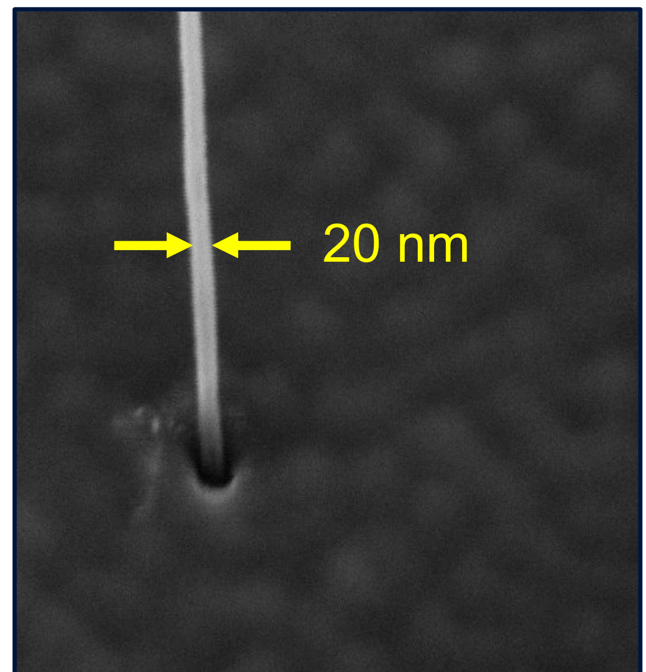


***Figure 11:** Single multi-walled carbon nanotube grown out of a nanohole in silicon dioxide. The diameter adjusts to the template diameter. A catalyst particle acts as growth center at the bottom of the hole.*

vias are prone to electromigration and subsequent failure in state-of-the-art metallization schemes, when exposed to high current densities. In Fig. 11 we show a single multi-walled nanotube that is grown out of a nanohole in SiO_2.
In Fig. 12 the electrical characteristic of such a structure is shown. Current densities up to 10^8 A/cm² have been applied without degradation or failure, well beyond the current densities in respective metal vias. The contact resistance of such a via is, however, still too high for applications.
The investigation of carbon nanotube vias is subject of the BMBF funded project “INKONAMI” which is performed in collaboration with the Max Planck Institut für Festkörperforschung Stuttgart.

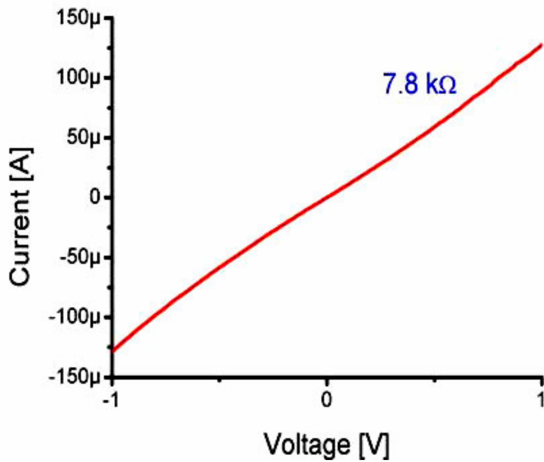


Figure 12: *Current voltage characteristic of a single multi-walled carbon nanotube via.*

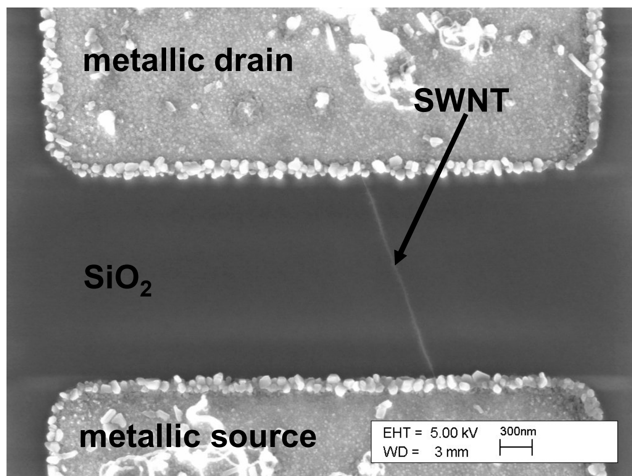


Figure 13: *Single-walled carbon nanotube contacted by two metal electrodes (top view). The silicon wafer acts as the back gate, separated by a* SiO_2 *dielectric layer.*

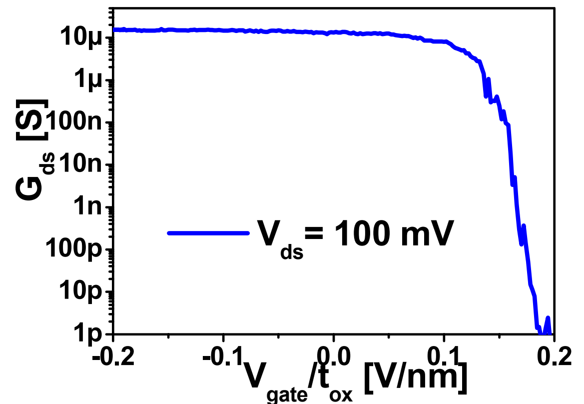


Figure 14: *Conductivity of the CNTFET in Fig. 13 as a function of the gate electric field. The p-type CNTFET can be switched off by more than 6 orders of magnitude.*

Carbon nanotube transistors

The first functional carbon nanotube field effect transistor (CNTFET) was published in 1998, two years before CPR NP started the carbon nanotube project. In 2002, we had our own first CNTFET with excellent features.
Fig. 13 shows a single single-walled nanotube grown by the catalyst-mediated CVD method between two metal electrodes. The source and drain electrodes and the tube are separated by a SiO_2 layer from the silicon substrate which acts as a back-gate. In Fig. 14 the conductivity of the tube is shown as a function of the electric gate field. It can be seen that the CNTFET can modulate the source/drain current by more than 6 orders of magnitude. This result also shows that nanotubes grown with a CCVD method compatible with microelectronics technology are of sufficient quality for applications. It should also be noted that nanotubes can be converted into the n-type modification by doping and that complementary arrays required for CMOS technology are possible.
It has been theoretically predicted that CNTFETs should perform much better than their silicon counterparts. The characteristics of current CNTFET demonstrators already compete in many aspects with state-of-the-art silicon transistors. However, CNT-“technology” is still in its infancy and far away from the mature silicon technology with regard to reproducibility and yield. However, CNT technology is progressing at a tremendous rate (more than 2400 publications last year) and Infineon is well positioned among the leaders in the field in terms of science and intellectual property.

Carbon nanotube power field effect transistors

At present, the growth of one sort of carbon nanotubes in a reproducible way remains a challenge. For application in transistors we require 100% single walled tubes with defined energy gaps of e.g. 1 eV. In addition, if we want to have a higher output current, we require ordered arrays of tubes, unlike the situation in silicon MOSFETs, where the gate area can be enlarged by lithographical methods. No such nanotube technology exists yet. However, we circumvent this unsolved problem by a proprietary concept where we deposit metallic and semiconducting tubes in a statistical way. Following a conventional one layer lithographic process to define source and drain on top of the nanotube layer, we apply a positive gate voltage to the back gate, driving the semiconducting tubes into depletion. Then, a voltage pulse is used to burn away the metallic tubes.
Fig. 15 shows a schematic of this device. Despite the uncontrolled nature of the deposition process, it was possible to produce transistors consisting of about 300 nanotubes that have a reasonable on/off ratio of 100 to 1000. Due to the ultimate current density in these tubes this device delivers output currents in the range of several milliamps, which is sufficient to driving LEDs or small electromotors (Fig. 16).

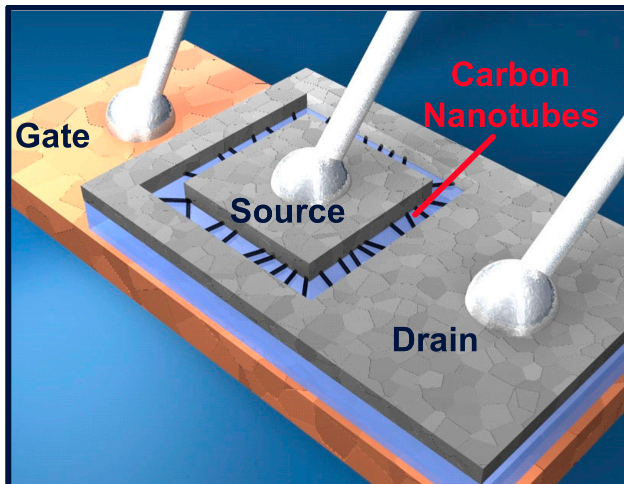


Figure 15: *Carbon nanotube power transistor.*

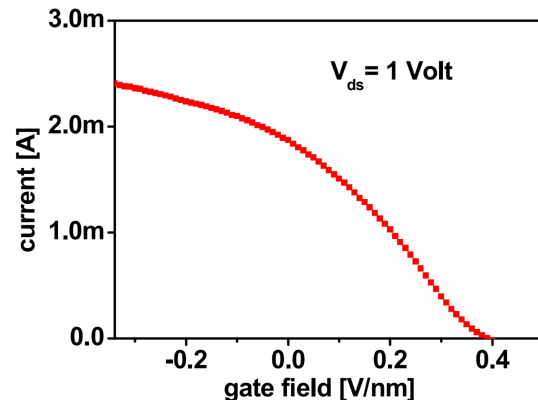


Figure 16: *Output characteristic of a nanotube power FET delivering 2.4 mA at 1Volt.*

This is the first time that these tiny nanotubes have been used to drive macroscopic loads, opening a new field of applications. Simply by increasing the channel area we might enhance the current by a factor of 10-100 and obtain devices with better characteristics than polycrystalline or polymer transistors. The fabrication of these devices is not restricted to silicon wafers but can be realized on any substrate, which is particularly useful for large area applications.

Dr. Franz Kreupl
Phone +49 89 234 44618
E-mail franz.kreupl@infineon.com

Dr. Georg Düsberg
Phone +49 89 234 55206
E-mail georg.duesberg@infineon.com

Dr. Andrew Graham
Phone +49 89 234 50271
E-mail andrew.graham@infineon.com

Dr. Mail Liebau
Phone +49 89 234 57433
E-mail maik.liebau@infineon.com

Dr. Eugen Unger
Phone +49 89 234 45132
E-mail eugen.unger@infineon.com

Dr. Wolfgang Hönlein
Phone +49 89 234 44397
E-mail wolfgang.hoenlein@infineon.com

Nano Devices

When will we reach the end of roadmap?

The minimum gate length of today's most advanced devices is about 40nm for high performance and 60nm for low power products with reduced off currents. The success of CMOS is based on scaling of the technology generations by a factor of 0.7 every three years. This makes the chips faster, reduces power dissipation and allows the integration of more transistors for complex functions at reduced costs. In the future, further down-scaling will become more difficult, especially for the mainstream bulk CMOS technology. Besides thinner gate dielectrics, higher doping concentrations and shallower junctions are needed to suppress short channel effects. However, this increases junction capacitance, junction leakage, parasitic resistance and degrades carrier mobility. Therefore, new device architectures will be needed to sustain the demands of the ITRS 03 [21] roadmap beyond the 45nm CMOS node which is expected for the year 2010.

Nanoscale Silicon transistors and memory cells

In a time frame of three to eight years ahead of production, the nano device group addresses the challenges of the roadmap with promising approaches for novel Si-MOSFETs with better electrical performance.
These are ultra thin SOI, multi-gate devices, and charge trapping memory cells. Multi-gate is regarded as the smallest possible silicon MOSFET. Two, three or four gates control in a very thin silicon channel the electrostatic potential much better than with a single gate. Moreover, the channel is isolated from the bulk using SOI material. We investigate two different architectures for multi-gate. The first is the FinFET type, which is highly compatible to bulk CMOS technology. It uses a 3d structure for the channel region surrounded by a gate. We demonstrated already n-and p-channel devices with tri-gate and good electrical characteristics down to 20nm. Our second and more innovative approach is a planar double gate transistor using wafer bonding. It is based on a fully depleted SOI transistor, where we achieved functional single gate devices with 25-16nm Si layers and adjusted threshold voltages. Due to the inherently shallow junctions, lower doping concentrations and lower junction capacitances, better electrical characteristics are typical for SOI compared with conventional bulk MOS-FETs. With wafer bonding as a new process module, recently we started to add a bottom gate to our ultra thin SOI transistor in order to get better channel control in planar devices. This architecture seems to be very suitable for the implementation of strained silicon layers with increased mobility for electrons and holes.
Our second key issue is a high density memory cell. We realized a small nonvolatile memory cell based on the tri-gate transistor but with an additional charge trapping layer as gate dielectric. Electrons can be injected by tunneling or hot carrier effects. Up to now, we succeeded to store two bits at a gate length of 100nm and one bit at 40nm with a threshold voltage shift of about 1V. Further progress is expected from thinner silicon channels.

Methods and team

For investigation of the new transistors and their performance we are processing demonstrators. We realize these small gates and active areas in our own cleanroom with e-beam lithography, resist techniques and nano analytical tools, like an atomic force microscope (AFM), high resolution secondary electron microscope (SEM) and focused ion beam (FIB). For patterning of the nano structures we are also developing etch processes on our dedicated etch reactor. All is compatible with the CMOS fabrication in MchP, where we run loops.
To support transistor processing and optimization we are involved in device simulations, ranging from drift diffusion to Monte Carlo. Another important issue for the very small devices is, to incorporate quantum mechanical effects like energy quantization, the quantum mechanical carrier distribution or tunneling effects for the prediction of the IV characteristics and the limits of the MOSFET.
Eleven researchers and two PHD students are involved in concepts for nanoscale transistors, memory cells, simulations, analytics and technology for demonstrators. We are confident that our research can give valuable inputs for the development of the platform technologies at CL and MP.

Dr. Lothar Risch
Phone +49 (0)89 234-44406
E-Mail lothar.risch@infineon.com

Nanoscale Si transistors

Objectives

As indicated by the ITRS roadmap scaling of conventional bulk CMOS transistors is becoming more and more difficult for the 45nm technology node and beyond. This is because ever higher doping concentrations in the channel and shallower junctions are needed in order to suppress the influence of the electric drain field at short gate lengths. Another critical issue is that probably high k dielectrics will be necessary with an equivalent oxide thickness below 1nm to achieve the desired on currents in the range of 1mA/µm at power supply voltages below 1V. Although several bulk transistors with extremely short channels have been demonstrated in the literature, they all suffer from lack of performance.

Therefore, novel transistor concepts for Si-CMOS are under investigation. One of the most promising candidates is Silicon on Insulator with an ultra thin Si layer of about 5nm to 10nm thickness [22]. Fig. 1 shows a schematic of such a device.

Due to the thin Si layer the influence of the drain voltage is reduced, the junction depth is extremely shallow and defined by the Si layer thickness. Moreover, the doping concentration in the channel can be low, resulting in improved charge carrier mobilities. Other advantages are the low body effect, reduced junction capacitance and a better subthreshold slope, because of the fully depleted body.

From device simulations we expect that about 20nm gate length with good electrical characteristics will become feasible, in accordance with the roadmap specs.

Beyond the single gate SOI transistor, devices with more than one gate can operate far beyond 20nm. It is commonly agreed that this architecture leads to the smallest possible MOSFET.

Several approaches have been proposed. Among them planar double gate devices, FinFETs and vertically surrounded gate transistors [23]. The FinFET type, shown in Fig. 2, offers a relatively simple process flow. A thin Si fin is surrounded by the gate and the current is flowing on the two vertical channels of the Si sidewall. Due to the two gates short channel effects are suppressed very effectively and the channel width of the device is independent of the lateral size.

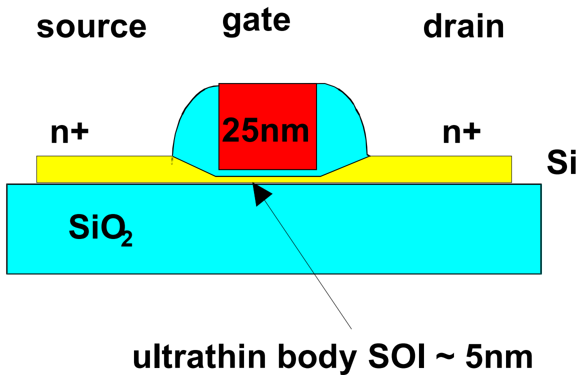


Figure 1: *Schematic cross section of an ultra thin SOI transistor with raised source drain.*

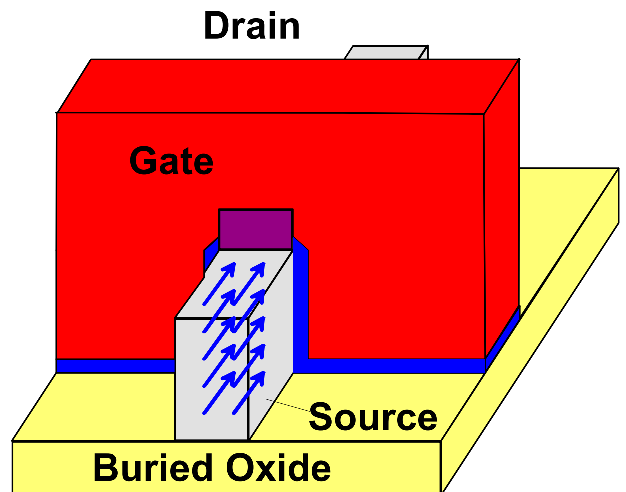


Figure 2: *Schematic cross section of a FinFET type double gate transistor.*

Results

Ultra Thin Film SOI Transistor

A CMOS compatible approach to solve many of the device problems due to short channel effects, shallow junctions and high doping concentrations is offered by Silicon on Insulator material. Several semiconductor companies already use SOI technology, especially for high performance microprocessors. Here the thickness of the Si layer is in the range of 60 to 100nm and the process flow and doping is similar to bulk devices. Despite some benefits, e.g. lower junction capacitance, these partially depleted SOI devices exhibit similar characteristics as bulk transistors. With regard to short channels much thinner Si layers are of interest. Reducing the Si thickness, the off current can be decreased to lower values even with an undoped channel and the subthreshold slope can come close to the ideal value of kTxln10=60mV/dec., where k is the Boltzman constant and T the temperature. Low doped channels are not feasible in bulk Si devices, because of punch through from source to drain. Without channel doping Zener tunneling currents are reduced and also electrical parameter variations due to statistical variations of the doping atoms. Moreover, the mobility of the charge carriers is higher in the low doped channels because of lower electric fields
The simulated electrostatic potential in an ultra thin SOI transistor with 25nm gate length is shown in Fig. 3 at a drain voltage of 1.1V. The gate voltage is 0V. A silicon layer of 10nm and a buried oxide thickness 100nm was assumed.

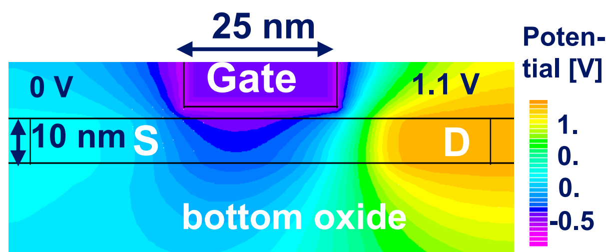


Figure 3: *Simulated electrostatic potential in a SOI transistor with 25nm gate and 10nm Si (Vgate=0V).*

The transistor can be turned off properly using such a thin silicon layer. Nevertheless, at the bottom of the silicon layer the gate potential is

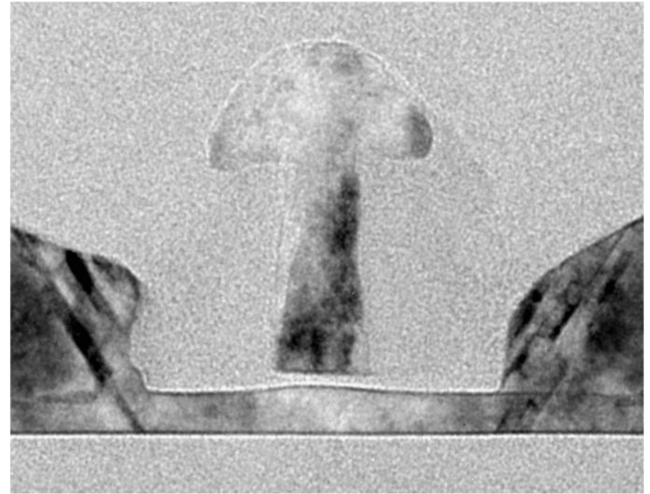


Figure 4: *TEM cross section of a SOI-MOSFET with 25nm gate length, Si thickness of 25nm, and epi layer for raised source drain.*

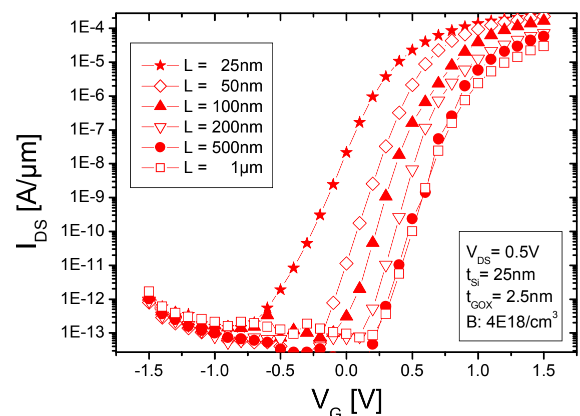


Figure 5: *I-V characteristics of n-channel SOI MOSFETs, tsi=25nm, tox=2.5nm.*

already slightly lowered. Thus for shorter gate lengths thinner silicon layers will be needed.
Fig. 4 shows a transmission electron microscope (TEM) cross section of a processed SOI MOSFET with 25nm gate. Here the body region of the transistor has still a thickness of 25nm. The poly Si gate was structured with our e-beam lithography and our Trikon etch tool in the CPR clean room. Raised source drain regions were grown with selective epitaxy for low resistivity contacts on the thin Si layer.
The measured I-V characteristics of a n–SOI MOSFETs with gate lengths down to 25nm [24] is depicted in Fig. 5.

Very good subthreshold slopes of 65mV/dec have been achieved down to the 50nm devices and 100mV/dec for the 25nm transistor. In the latter, due to the relatively thick Si layer of 25nm short channel effects cannot be suppressed completely. This has been also indicated in the simulation in Fig. 3, where even at a Si thickness of 10nm low currents start to flow at the bottom of the Si layer. As a simple rule, for good electrical parameters the silicon thickness should be 3-4 times smaller than the gate length [25], [26].
Focussing on e-beam lithography, we can already process much smaller devices. In Fig. 6 a top view on a device with 13nm gate length is

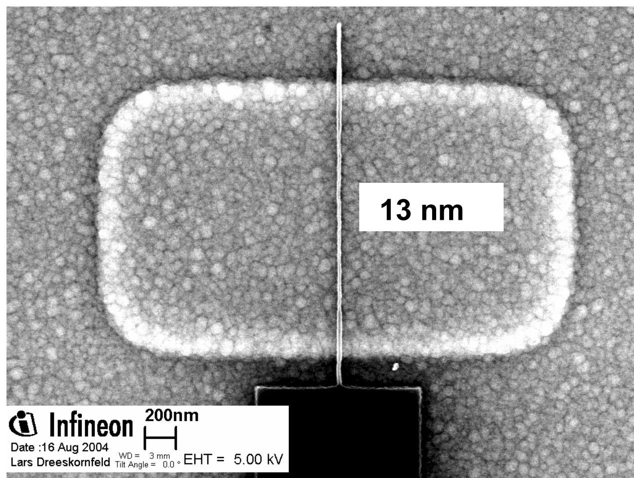


Figure 6: *SEM top view on a SOI transistor with 13nm gate exposed with e-beam litho (in resist).*

given. With thinner Si layers we expect functional SOI devices below 20nm gate length.

Dr. Jessica Hartwich
Phone +49 (0)89 234-45728
E-Mail jessica.hartwich@infineon.com

Tri-gate transistor

Further reduction of the gate length will need multi-gates together with thin Si layers for the control of the channel [27], instead of only a single gate. The advantage of the multi-gates is to suppress the influence of drain electric field on the channel more effectively [28]. Moreover, the silicon thickness can be relaxed and the on-current is doubled, for example, when the current is flowing in two channels created by the gate at Si sidewalls. The challenge for multi-gate transistors will be, to develop a reliable process for production. This is not an easy task. Another

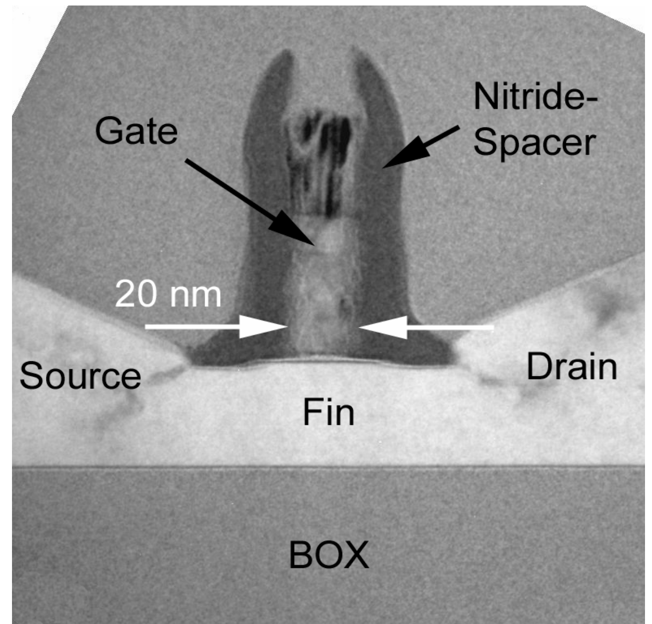


Figure 7: *TEM cross section of a 20nm tri gate device on buried oxide with raisede source drain regions.*

issue are self aligned source drain regions to the gate for fast switching speed.
The FinFET structure can realize this with relatively simple processing steps [29]. Two channels are located at the sidewalls of a thin silicon fin. For the tri-gate device also the planar top of the Si layer is used as a channel region. Thus the gate controls the charge carriers very effectively from all sides. Compared to the ultra thin SOI transistor, the tri-gate device requires two demanding lithography and etch process steps. The definition of the channel region including the source and drain contacts is the first process step, where the control of the fin width and steep etching profiles are of great importance.
A TEM cross section along the fin of a processed tri-gate device is given in Fig. 7. Typical fin widths are in the range of 15 to 30nm and the gate length is 20nm. Raised source drain regions are used for the contacts, which are very difficult on thin Si layers. The gate is protected with an oxide nitride spacer against shorts to source and drain during epi growth and serves also as an implantation mask for the self aligned source drain regions.
Fig.8 shows a TEM cross section across a small fin processed with rounding oxidation to avoid thinning of the gate dielectric at the corners. The heigth of the fin is about 40nm and the thickness on top is 35nm and 17nm at the bottom.

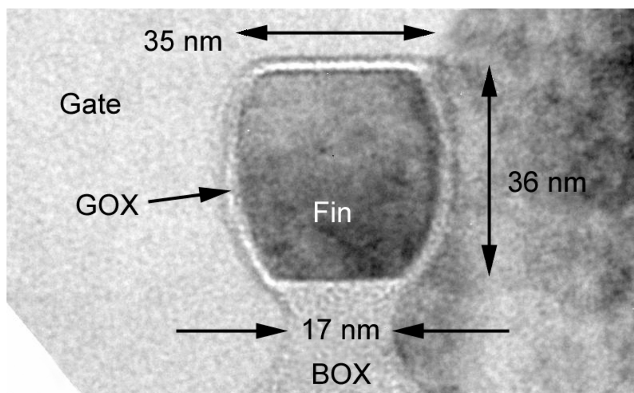


Figure 8: *TEM cross section of a 17-35nm thick Si fin with 36nm height on buried oxide for a tri-gate MOSFET. The thickness of the gate dielectric is 3nm.*

Our thinnest fins are in the range of 15nm, suitable for gate lengths of 15-25nm.
The measured I-V characteristics for a tri-gate device with 20nm gate length is given in Fig. 9. For the n-channel an on-current of 1350µA/µm at an off-current of 70nA/µm has been measured at 1.2V power supply voltage. The current is normalized to the fin height. Remarkable is the high drive current taking into account the relaxed oxide thickness of 3nm.
With lower threshold voltage we reached an on current above 1500µA/µm.
Also p-channel tri-gate devices have been successfully realized. The p-channel device is more difficult than the n-channel because of the enhanced diffusion of the highly boron doped source drain regions while arsenic is used for the n-channel. Here we achieved with 30nm gate length an on current of 500µA/µm at 1.2V together with an off current of 2nA/µm.

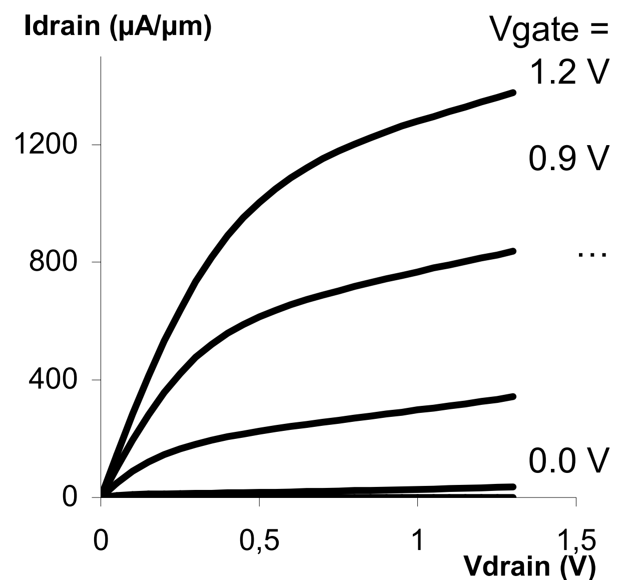


Figure 9: *Measured I-V characteristics of a tri-gate MOSFET with 20nm gate length at 1.2 V power supply voltage, tox= 3nm.*

Fig. 9 Measured I-V characteristics of a tri-gate MOSFET with 20nm gate length at 1.2V power supply voltage, tox= 3nm
Currently, tri-gate devices with an gate oxide thickness of 2nm are under processing. From the thinner gate dielectric further improvement in drive current can be expected.

Dr. Wolfgang Rösner
Phone +49 (0)89 234-49118
E-Mail wolfgang.roesner@infineon.com

High density memory cells

FinFlash nonvolatile data storage

The increasing demand for mobile applications such as digital cameras, camcorders, MP3 players or PDAs requires storing of large amounts of data on flash memory cards or USB sticks. These key applications drive the spectacular 30% annual growth of the nonvolatile data storage market predicted for the next four years (see Fig. 10). Currently, the floating gate cell in high density NAND arrays is the state-of-the-art technology. Operated in multi -level mode this technology is very cost competitive and expected to be scalable at least down to the 50nm node in ~2007. Below 50nm the most challenging scalability issues are the isolation of floating gate to floating gate interference between adjacent word lines and the electrostatic gate control of the channel region for small gate lengths.

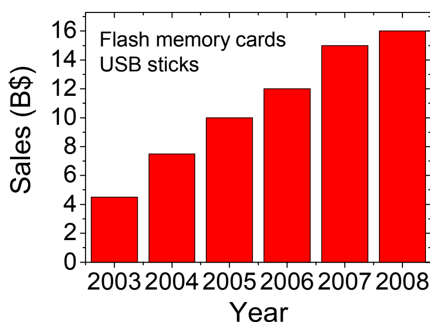


Figure 10: *Market evolution for flash non-volatile memory cards and USB sticks. A strong 30% average annual growth is predicted for the next four years. (iSuppli).*

As an alternative to NAND floating gate, Infineon Flash has recently introduced the TwinFlash charge trapping technology based on a 2-bit storage in a single cell that has just started to enter the data storage market. It is expected that 2-bit storage is scalable for several technology generations and thus will coexist as a cost effective solution with floating gate NAND for the next few years.

FinFlash for single bit storage

Facing the scaling issues for the sub-50 nm range, Corporate Research presented at this years' VLSI (Very Large Scale Integration) Symposium in Honolulu novel FinFET based charge trapping memory cells suitable for very high integration densities [30]. Similar as in logic applications these new memory transistors make use of a gate that surrounds a Si-fin

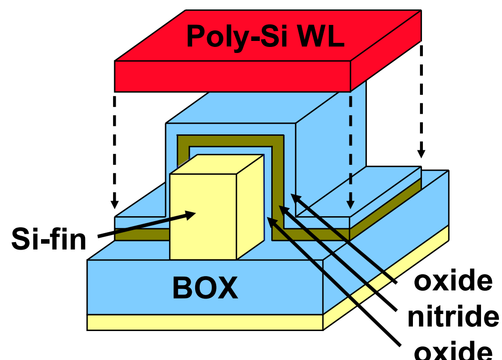


Figure 11: *Novel FinFET devices with nitride trapping dielectric for non-volatile data storage. Information is stored by uniformly injecting charge into the trap rich nitride layer.*

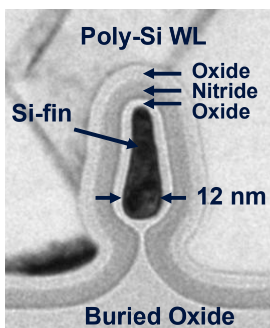


Figure 12: (a): *Transmission electron micrograph of a processed FinFET device showing the Si-fin surrounded by the oxide-nitride-oxide dielectric layers and the poly-Si tri gate. The charge is stored in the silicon nitride trapping layer.*

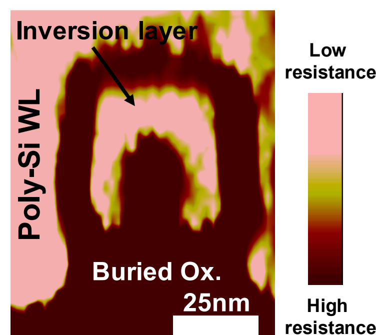


Figure 12: (b): *High resolution scanning spreading resistance micrograph of a FinFET device in the On-state. The bright zones indicating highly conductive regions at the three sides of the silicon fin reveal the inversion layer.*

(see Fig. 11) to improve the electrostatic channel control and thereby their scalability. The charge is uniformly injected and stored in a nitride trapping layer that is adjacent on the three sides of the fin. Compared to floating gate cells the tunnel oxide has improved scaling properties since trapping layers are less sensitive to single leakage paths than floating gates. With this device architecture, CPR achieved memory transistors (see Fig. 12) with very short gate length down to 30nm using fin widths as small as 10-20nm on SOI substrate. Threshold voltage shifts of 1.5V at NAND compatible program and erase times were realized (see Fig. 13 top). These device architectures were also investigated by 3D drift-diffusion simulation demonstrating the very good scalability of these tri-gate devices even below 30nm (Fig. 13 bottom).

If operated in a 4-5F² high density array such as NAND this would enable memory densities up to 16Gbit per die. This is about a factor of 10 above the currently available densities in single-level operation. With even smaller fins the gate length and thus the technology is expected to be further scalable down to the F=25nm node ultimately limited by the thickness of the two oxide-nitride-oxide layers in between the fins (see Fig. 14). In addition, this technology does not require any new materials and is therefore fully compatible with well known CMOS processes. Body tight FinFETs can also be fabricated on bulk Silicon.

As a high density array for these FinFET memory transistors a NAND (see Fig. 14) as well as a NOR organization have specific advantages and challenges. NAND provides simpler processing as well as highest density while having the drawback of challenging read and write disturb requirements and slow serial access. We have successfully optimized the oxide-nitride-oxide dielectrics for threshold shifts in the 1-2V range in order to meet these array imposed disturb constraints. In contrast, NOR for highest densities uses more complex processing but allows for relaxed disturb properties of the memory transistors and thus larger threshold shifts and fast access. The choice will be ultimately governed by an optimization of access time, cost per bit and yield.

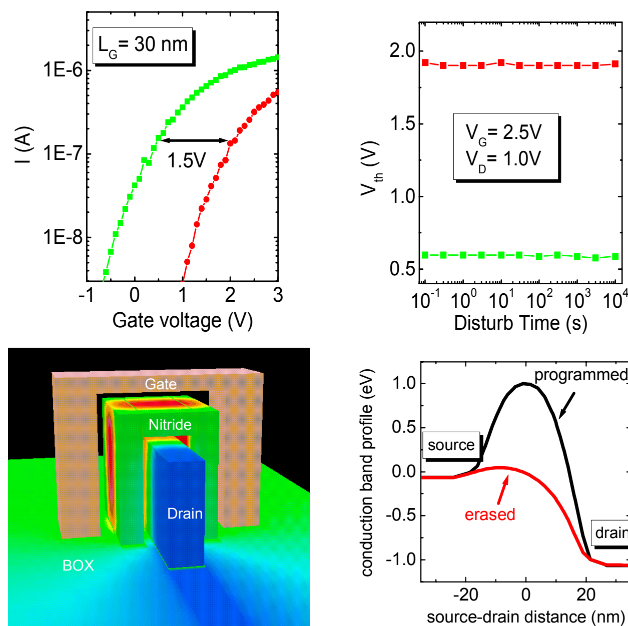


Figure 13: *Top left: Transfer characteristics of a processed tri-gate oxide-nitride-oxide transistor with a gate length of L_G = 30 nm. Programming and erase parameters are 12.5 V at t_P = 500 µs and -11 V at t_E = 2 ms. Right : Read disturb measurement indicating robust retention properties. Bottom left: 3D drift-diffusion simulation showing potential contours in the programmed state. Right : Cross sectional view along the fin axis between source and drain.*

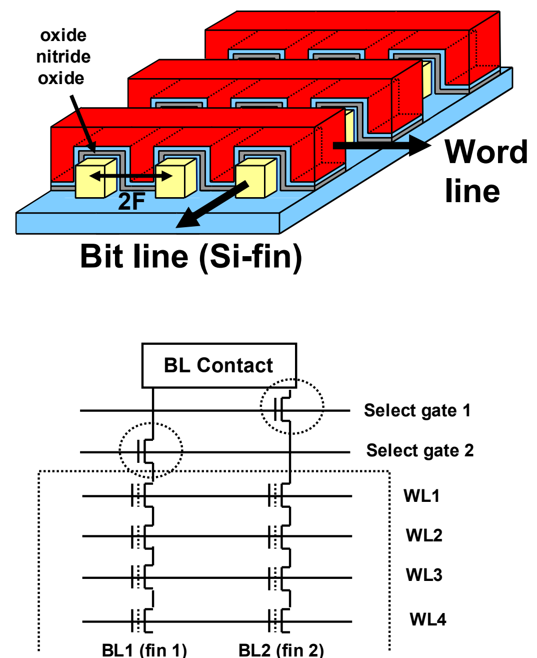


Figure 14: *Top : Schematic 3D view of a NAND type array organization with word lines (WL) perpendicular to the Si-fin. Bottom : NAND type array with two select transistors allowing for large bit line contact areas.*

FinFlash for two bit storage

The basic idea of two-bit storage in planar transistors is illustrated in Fig. 15. Charge is injected by hot electrons and stored locally close to the drain p-n junction in a nitride storage layer. Due to the symmetry of the cell another bit can be stored at the source junction by simply using opposite programming voltage conditions at source and drain thus enabling two bits in a single cell. Erasing occurs by injecting hot holes at each p-n junction. Reading selectively bit 1 requires a typical voltage V_D = 1.5V at the source contact, in reverse mode compared to programming. Bit 2 is read analogously, but in opposite mode.

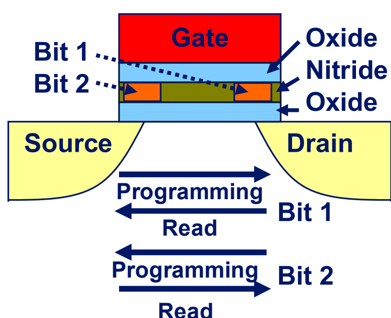


Figure 15: *Dual-bit storage in Infineons TwinFlash oxide-nitride-oxide memory cell.*

The most critical issues for scaling of the planar dual - bit TwinFlash cell are punch-through control due to the strong fields between source and drain during programming as well as lateral charge leakage. In order to improve the electrostatic gate control of the channel region and better screen source-drain fields we investigated the tri-gate oxide-nitride-oxide devices also for two bit storage (Fig. 16). Here, programming and erasing occurs in close analogy to the planar variant and charge is stored at the three sides of the fin close to the p-n junctions of source and drain.

We achieved good bit separation for gate lengths of 100nm (Fig. 17) with low drain voltages of V_D = 3.9V and a programming time of t_P = 10μs. Since the drain voltage is below the punch-through voltage for this gate length this dual bit FinFET approach is promising for improved punch-through control in a commonly used virtual ground array.

Conclusion

We have introduced and fabricated novel FinFET based nonvolatile charge trapping cells.

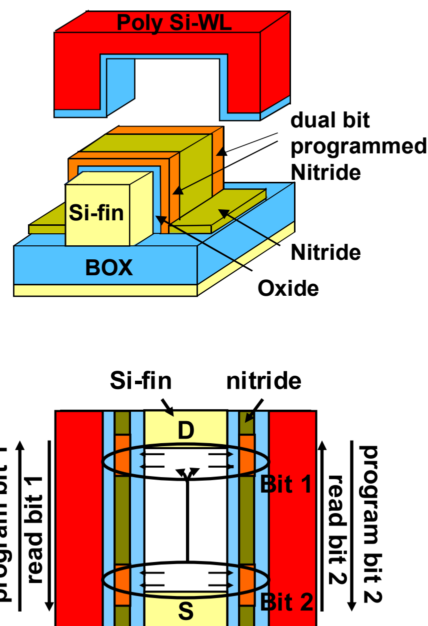


Figure 16: *Top: FinFET oxide-nitride-oxide memory cell operated in dual bit mode. Charge is stored at the three sides of fin close to the p-n junctions of source and drain. Bottom : Top cross sectional view of the devices operated in dual bit mode. The programming and reading occurs analogously to the planar dual-bit devices.*

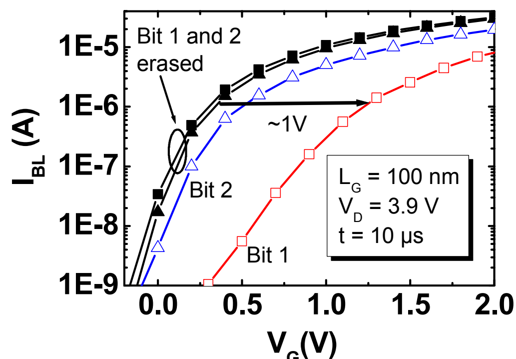


Figure 17: *Transfer characteristics of a fabricated FinFET oxide-nitride–oxide memory cell demonstrating dual bit operation. The ONO dimensions are 3nm / 4nm / 5nm. Bit 1 is programmed (red) without significantly affecting the read characteristic of the erased state Bit 2 (blue).*

These devices operated in single bit mode are scalable well below the 50nm node and thus are suitable for very high density data storage. Such a technology could replace NAND floating gate for F < 50nm in 2007. FinFET oxide-nitride-oxide cells operated in dual-bit mode offer promising behaviour for gate lengths as small as 100 nm and therefore are currently under further investigation.

Michael Specht
Phone +49 (0)89 234-40214
E-Mail Michael.specht@infineon.com

Advanced Mixed Signal Applications

Introduction

As the interface between human senses and many other signal sources and electronic circuitry is of analog nature, analog CMOS circuits represent an important part of today's systems-on-a-chip. There, the integration of the required analog circuits together with digital data processing blocks results in chips with signal representations in mixed domains. However, also the behavior of classical digital circuits needs to be considered from an analog perspective, when aiming for circuit optimization concerning particular parameters such as operating power vs. speed, standby-power etc.
Modern CMOS processes usually offer a number of different types of transistors, whereas high-speed optimized devices e.g. show relatively high leakage currents in the off-state or standby-mode. Sole use of low-leakage devices, however, may lead to delay penalties in a given circuit. For that reason, our department is working on library cell approaches which allow optimization of both parameters within a corridor representative for Infineon's product portfolio. Moreover, it is our goal to fully exploit the properties of state-of-the–art CMOS processes to push analog circuits' performances to their limits.
The expression "Applications" in the name of this department on the other hand emphasizes, that we used our knowledge on mixed-signal circuit design not only within classical areas as discussed above, but also to solve application-driven requirements. In particular, we were aiming for user-friendly system integrations of CMOS-based biosensor arrays. For that purpose, we used relatively inexpensive standard CMOS processes with larger feature sizes as compared to most advanced technologies, but equipped these processes with extra processing steps to provide the required transducer layers, and developed sophisticated high-precision analog circuitry specifically adapted to the sensor principles used.

Dr. Roland Thewes
Phone +49 (0)89 234-41964
E-mail roland.thewes@infineon.com

A 4GS/s 6b Flash ADC in 0.13µm CMOS

Today's high data transfer rates in many serial communication lines such as disk read channels and data networks profit from digital signal processing circuitry. In such systems, high speed ADCs are required to provide the interface between the analog and the digital world. Moreover, an "analog character" of binary signals is also obtained in some applications due to distortion and attenuation within transmission channels.

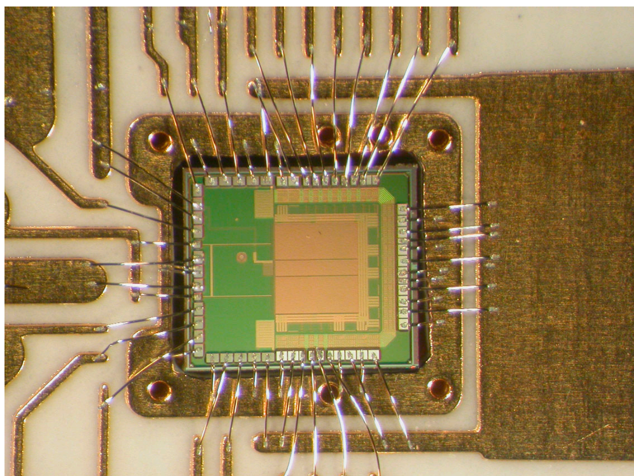


Figure 1: *Microphotograph of the ADC on a RF test board.*

It is desirable to realize the required ADCs in standard CMOS technology to allow low cost production and monolithic integration of ADC and digital signal processors. In recent publications time interleaving of several ADCs was used to realize sampling rates in the multi-GHz range. In this article a 6b 4GS/s flash ADC realized in a standard 0.13µm n-well CMOS technology is presented featuring an averaging scheme in the digital domain and 8b output.

Device Mismatch Issues

The mismatch of integrated circuits strongly depends on the active area of the devices used, according to the relation $\sigma_p = c_p/(W \cdot L)^{1/2}$. There, σ_p is the deviation of the electrical parameter p, c_p is the process specific matching constant, and

W and L are width and length of the active area of the device. This relation holds for many analog parameters of different devices, e.g. MOSFET threshold voltage V_{th} and resistance R of poly-Si resistors. Therefore, to meet the offset requirements for the input voltage of comparators, the related devices have to be sized accordingly. Due to the reduced supply voltages in modern CMOS processes and comparatively large threshold voltages, the input voltage range of the comparators is limited which aggravates the matching restrictions in such systems. In our approach we relax the matching requirements referred to a single comparator by using a fourfold larger number of comparators as would be necessary for the aspired resolution of the flash ADC. The statistical averaging of the comparator results is then performed in the digital domain.
As a result, we gain more freedom in the design and the physical layout of the comparator, resulting in a higher conversion speed of the comparators.
The new architecture does not reduce the total area of the comparator bench or reduce its power consumption, but higher sampling speeds can be realized with smaller sized comparators.

ADC Architecture

The basic idea behind the new concept is illustrated in Fig. 2. In a classical n bit flash ADC, 2^n-1 comparators with low input offset voltages are used to generate a perfect, bubble-

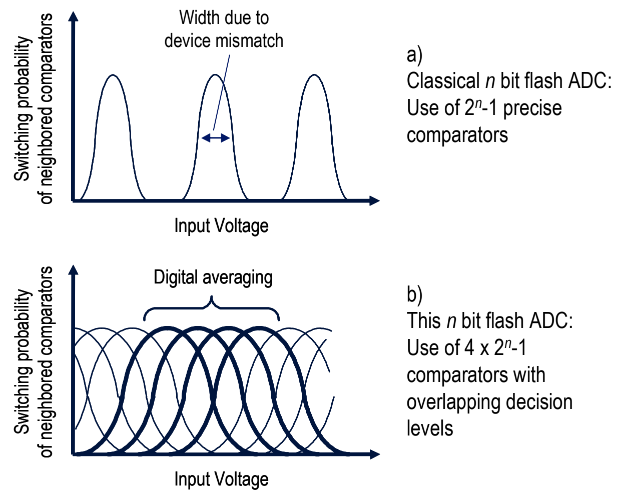


Figure 2: *Illustration of the ADC operation scheme.*

free thermometer code at the output of the comparator bench. To guarantee the demanded low input offset voltage, large active device areas must be used to reduce the effect of device mismatch within the comparators.
In our realization, aiming at an ADC with 6b linearity, 4×64-1=255 (=2^{6+2}-1) comparators with small active area are used. As a result, the input offset voltages are higher. Consequently, a bubble-free thermometer code at the output of the comparator bench is not obtained, but the small sized comparators can be optimized for maximum operation speed. Device mismatch related errors in the code at the output of the comparator bench are compensated by averaging in the digital domain which can be

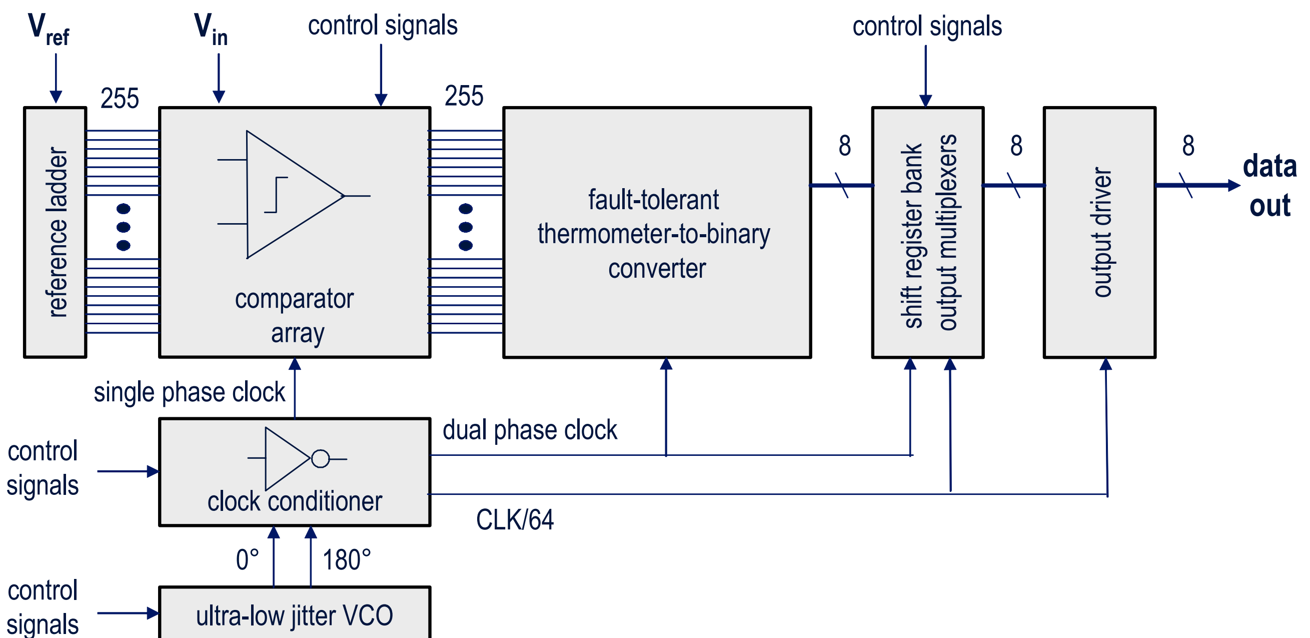


Figure 3: *Architecture of the ADC.*

accomplished at highest speeds.
Fig. 3 shows the schematic block diagram of the proposed high speed ADC. As described before, the comparator array consists of 255 units. The reference voltages are generated by a resistive ladder. Since clock jitter directly translates into a loss of the ADC's resolution, an on-chip LC-oscillator with low phase noise is used. The differential sinusoidal output of the oscillator is amplified, and provided to the comparators and to the thermometer-to-binary converter. To ensure a constant delay of the clock signal applied to all comparators, the clock is distributed by means of an H-tree.
The comparator outputs are connected to a fault-tolerant thermometer-to-binary converter with an 8b output. Since at this point the data rate is 4GB/s, for test purposes a multiplexer is provided on-chip which transmits every 64th digital word to the output of the chip. The obtained signals are then recorded by a logic analyzer.

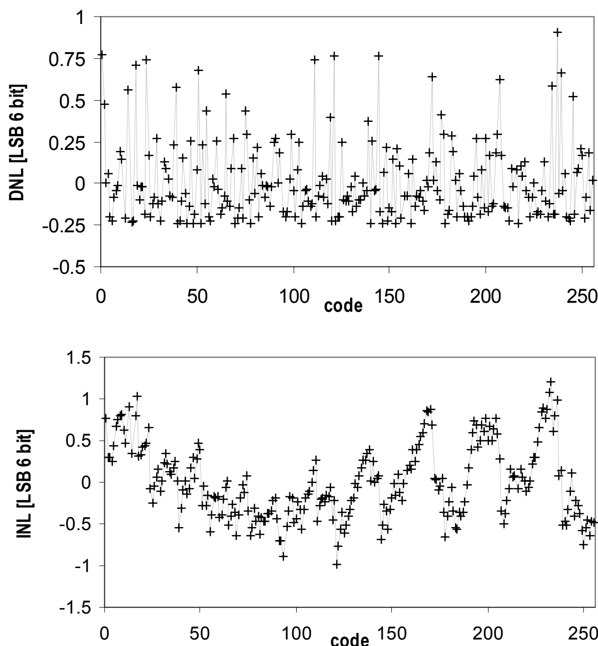


Figure 4: *Differential (upper plot) and integral nonlinearity (lower plot) of the ADC.*

Measured Results

The measured DNL and INL of the ADC are given in Fig. 4. Both diagrams show the nonlinearities related to the LSB of the 6b output signal. The results of the DNL clearly show the statistically varying offset voltages of the

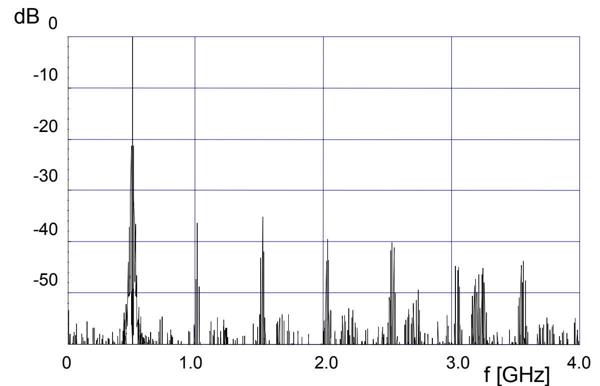


Figure 5: *Spectrum of the ADC output at fin=509MHz, fCLK=4GHz.*

comparators. As a result of the architecture of this ADC, errors in monotony cannot occur.

Table 2: Measured performance data of the ADC.

Process	0.13µm, 1P6M, digital CMOS
V_{DD}	1.5 V
Clock frequency	4.0 GHz
Resolution	6 bit (8 bit output)
DNL	-0.23 / +0.91 LSB
INL	-0.98 / +1.2 LSB
SFDR@f_{in}=509 MHz	36 dB_{FS}
SFDR@f_{in}=1017 MHz	30 dB_{FS}
Input voltage range	0.6 V
Power consumption @ f_{CLK}=4 GHz	990 mW (900mW digital, 90mW analog)
Chip area	4.6 mm² (0.5 mm² active area)

Dynamic measurements reveal proper operation of the ADC up to input frequencies of 1GHz at a sampling rate of 4GS/s. Fig. 5 shows the measured spectrum of the ADC output at an input frequency of 509MHz. A spurious free dynamic range of 36dB_{FS} is obtained. The performance data of the ADC are summarized in Tab. 1.
A microphotograph of the chip bonded onto the RF-PCB is shown in Fig. 1.

Conclusion

In the 6b 4GS/s Flash ADC described here, only standard digital MOSFETs are used, which allows to monolithically integrate it in a signal processor without the need for analog process options. The RF clock signal is generated on-chip and only a single supply voltage of 1.5V is used.

Christian Paulus
Phone +49 (0)89 234-41703
E-mail christian.paulus@infineon.com

Technology-Oriented Circuit Design Techniques for Low Power Nanometer-Scaled CMOS

Power Challenge in sub-100 nm CMOS

The dramatic increase of active and leakage power dissipation is one of the major challenges for sub-100 nm CMOS circuits. In particular, for portable applications, such as cellular baseband chips, MP3 players, and especially for future applications in the field of ambient intelligence the power budget is restricted by the battery capacity. Fig. 6 shows the power dissipation of a generic system-on-chip based on ITRS data. Within ten years or four CMOS technology nodes (130 nm to 45 nm), leakage power increases by about three decades. Thus, power reduction techniques are increasingly required for CMOS circuit design. Although various power reduction techniques have been proposed recently, their successful implementation strongly depends on device properties. Therefore, a thorough choice of device options is a prerequisite to leakage aware circuit design. The sensitivity of sub-100 nm CMOS devices to parameter variations is an additional challenge for circuit design as illustrated by the increased leakage currents in Fig. 6 if statistical parameter variations are considered. This motivates the introduction of statistical-based design methodologies into the design flow to estimate the effect of variability on the circuit behavior.

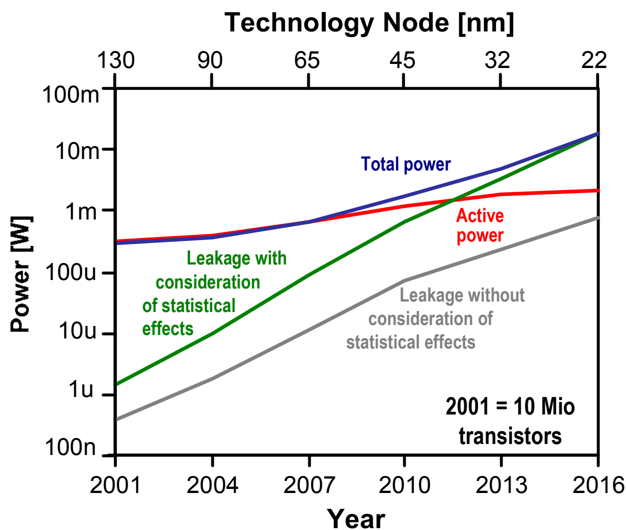


Figure 6: *Active and leakage power per chip at constant die size for low standby power logic devices (ITRS 2003). Switching activity factor is 0.001.*

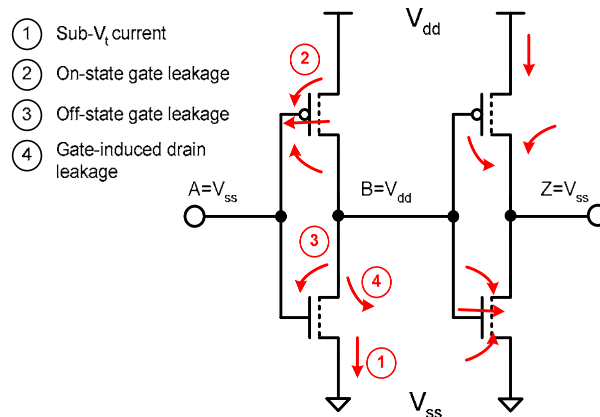


Figure 7: *Leakage currents in sub-100 nm CMOS circuits.*

Sleep Transistors and Body Biasing

Fig. 7 illustrates the different leakage currents in a simple CMOS inverter pair. In 90 nm CMOS technology and beyond, gate leakage currents are a substantial part of the total leakage. The use of sleep transistors represents an attractive approach to disconnect inactive circuit blocks from the power supplies during standby mode (Fig. 8). In particular, gate leakage currents are eliminated if special low-leakage devices with thicker gate oxides (t_{ox}=2.2 nm) are used for the sleep transistors. In this way, the large leakage currents of fully scaled logic core devices with

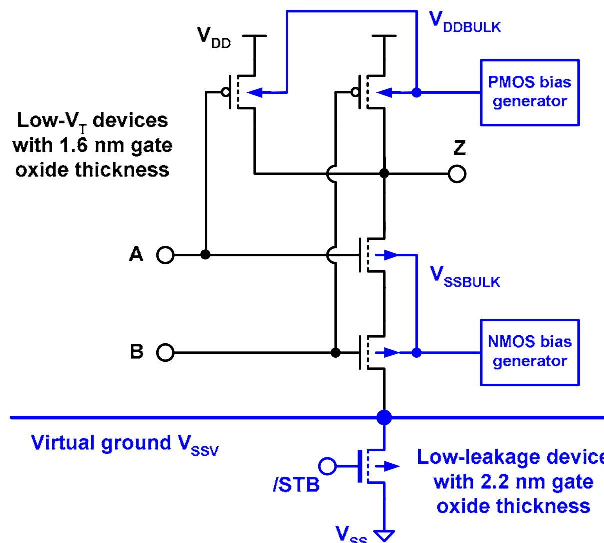


Figure 8: *Sleep transistor technique and body biasing applied to a CMOS NAND logic gate.*

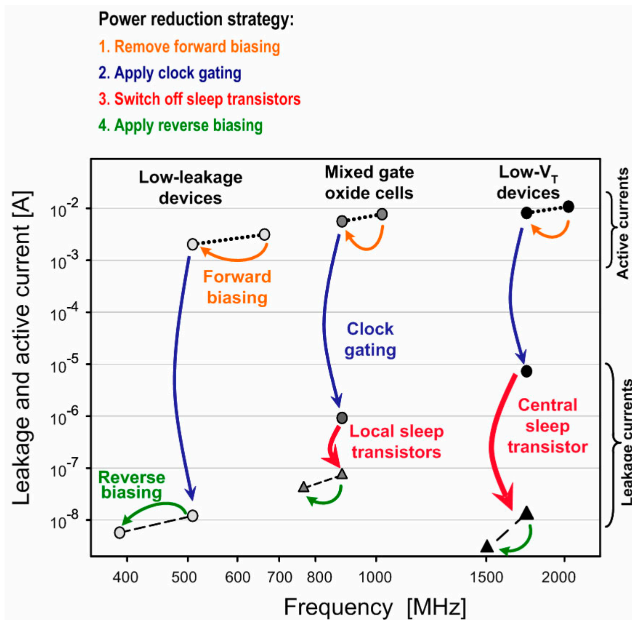


Figure 9: *Measured leakage-performance trade-off for three 32 bit adder cores implemented with different device options in 90 nm CMOS technology at V_{DD} = 1.2 V and T = 25 °C.*

thin gate oxides (t_{ox}=1.6 nm) are eliminated. Low power optimized CMOS processes typically offer such devices.

Body biasing is a further design methodology to adapt a circuit block to different operating conditions. To improve the circuit performance during active operation, forward bias voltages are applied to the body contacts of NMOS and PMOS devices [34]. Forward biasing reduces the threshold voltages and thus increases the on-currents of the devices. Applying reverse bias voltages raises threshold voltages, thereby reduces the sub-threshold currents, and thus saves power in the standby mode.

Experimental Results: 32 Bit Adder Cores

To evaluate the benefit of power reduction techniques for representative logic circuits, three 32 bit adder cores have been fabricated in a 90 nm CMOS triple-well technology using different device options. The adder cores have a logic depth of nine stages and a circuit complexity of about 5000 transistors including clock distribution circuitry and flip-flops. Fig. 9 illustrates the leakage-performance trade-offs for the adder cores [35]. Following power reduction schemes are implemented: classical clock gating, body biasing, and sleep transistors.

During active mode, a 0.5 V forward bias voltage improves the circuit speed. The observed performance increase is 13 % for the adder composed of low-V_T devices. A maximum performance of 2 GHz frequency is demonstrated. For the adder composed of low-leakage devices, forward biasing is even more efficient and improves the speed by 35 % from 500 MHz to 660 MHz. For medium performance requirements, a novel circuit scheme based on 1.6 nm and 2.2 nm gate oxide devices for logic gates is implemented. Here, local sleep transistors are used within a logic gate to enable a fast reactivation of the circuit from standby mode. The low-V_T adder version has a central sleep transistor with better leakage reduction capability but a longer reactivation time.

During standby mode, forward bias is first removed (orange arrows). Then clock gating is applied to eliminate the active power dissipation in the clock distribution circuitry and in the flip-flops (blue arrows). Depending on the device options, the power dissipation is reduced by three decades for low-V_T devices and five decades for low-leakage devices. Switching off the sleep transistors (red arrows) reduces the leakage current to 70 nA for the adder composed of mixed gate oxide cells and to 12 nA for the low-V_T adder. Especially the results obtained for the low-V_T adder indicate that the sleep transistor technique is mandatory for future technology generations. If a 0.5 V reverse bias voltage is applied to the adder cores, the measurement results clearly show that reverse biasing is the least efficient leakage reduction technique for the investigated 90 nm CMOS technology.

Dr. Christina Pacha
Phone +49 (0)89 234-57442
E-mail christian.pacha@infineon.com

Klaus von Arnim
Phone +49 (0)89 234-54411
E-mail klaus.vonarnim@infineon.com

Dr. Ralf Brederlow
Phone +49 (0)89 234-50575
E-mail ralf.brederlow@infineon.com

From Feasibility Studies to Prototype Design: The Infineon CMOS DNA Chip

Together with partners from the Fraunhofer Institute for Silicon Technology (Itzehoe) and from Siemens, two years ago Corporate Research presented first results concerning a CMOS-based fully electronic DNA sensor array chip [36-37], developed within the framework of a project funded by the Bundesministerium für Bildung und Forschung, Germany. Meanwhile, a customer-oriented chip version is available suitable for robust application in user-friendly integrated systems [39].

Detection principle and CMOS integration

The DNA detection method used [38] is briefly reviewed in Fig. 10. We use interdigitated gold electrodes and an enzyme-label based current generation process.

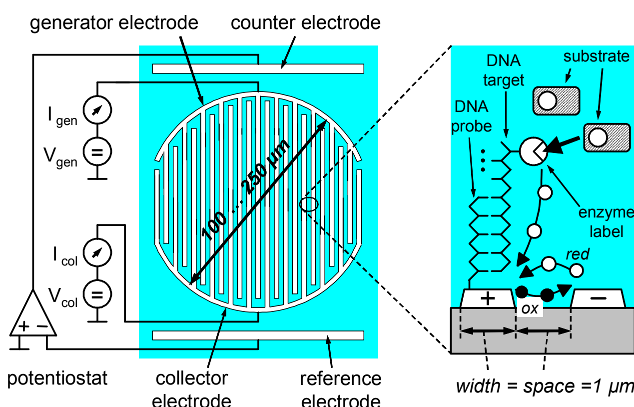


Figure 10: *Schematic plot showing the redox-cycling sensor principle and the sensor layout. Left: Single sensor consisting of interdigitated gold electrodes and a potentiostat circuit with counter and reference electrodes. Right: Blow-up of a sensor cross-section showing two neighboring working electrodes after successful hybridization. For simplicity, probe and target molecule are only shown on one of the electrodes.*

Probe molecules are immobilized on the gold surface. The target molecules in the analyte are tagged by an enzyme label (Alkaline Phosphatase). After hybridization and washing phases, a substrate (para-Aminophenyl-phosphate) is applied which is cleaved by the enzyme label, so that electrochemically active compounds (para-Aminophenol) are generated at the sites with matching DNA strands. Applying simultaneously an oxidation and a reduction potential to the sensor electrodes (V_{gen} and V_{col}, e.g. +300 mV and –100 mV), a redox process occurs at the electrode surfaces which translates into electron currents at the electrodes (I_{gen} and I_{col}).
As shown in Fig. 11, the required noble metal sensors are integrated into a 6", 0.5 µm, 5 V, n-well CMOS process [36, 37].

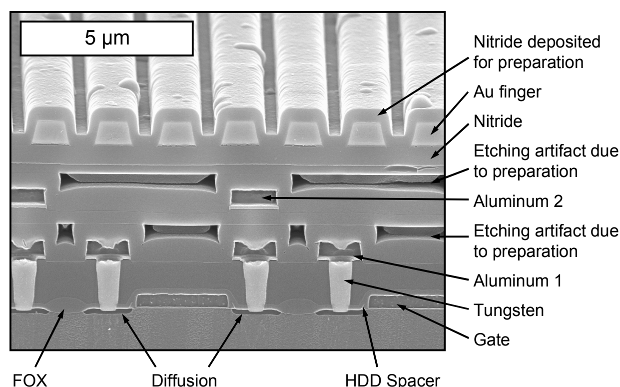


Figure 11: *Tilted SEM cross section photograph of the extended CMOS technology with Au sensor electrodes and CMOS elements after the complete process run [37]. Note, that the nitride layer on top of the sensor electrodes is only used for preparation purposes.*

DNA-detection-system-on-a-chip

Recently, a full DNA-detection-system-on-a-chip was presented [39] (Fig. 12). These chips consist of a sensor array with 8 x 16 sensor sites, in-sensor site current-mode A/D conversion, and on-chip peripheral circuitry including bandgap and current references and autocalibration circuits, D/A-converters to provide the required voltages for electrochemical operation, and a serial digital electronic interface with a total of six pins for power supply and data transmission.
An innovative packaging solution and a user-friendly readout apparatus including software for analysis are under development as well.

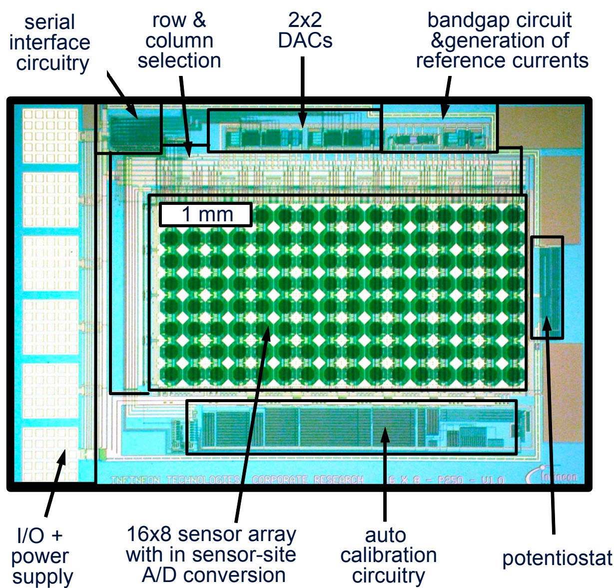


Figure 12: *Photo of a prototype array chip with 16 x 8 positions, 6 pad pure digital electronic interface, and comprehensive electronic functionality on-chip.*

In sensor-site current mode A/D conversion

As in former approaches with fully analog sensor-site circuitry [36, 37], the in-sensor site A/D conversion approach [40] provides a specified dynamic range of five decades, i.e. 10^{12} A … 10^{-7} A current resolution.. However, compared to analog sensor site circuitry the digital solution leads to increased robustness of the data transmission within the array. Moreover, it allows to sample the data from all sites simultaneously which is in particular advantageous for chips with a larger number of test sites.

The principle of the specifically adapted analog-to-digital converter is shown in Fig. 13. The voltage of the sensor electrode is controlled by a regulation loop via an operational amplifier and a source follower transistor. For A/D conversion, a current-to-frequency converting sawtooth generator concept is used, where an integrating capacitor C_{int} is charged by the sensor current. When the switching level of the comparator is reached, a reset pulse is generated which passes through a delay stage, and the capacitor is discharged again by switch transistor M_{res}. The delay stage is required as a pulse shaping unit to ensure a sufficient length of the reset pulse applied to M_{res} so that complete discharging of the integrating capacitor is guaranteed.

The frequency behavior as a function of the sensor current including parasitic and device mismatch effects is approximated by:

$$f \approx I_{sensor} / (C_{int} \times V_{sw\text{-}th})$$

There, f is the oscillation frequency, $V_{sw\text{-}th}$ the comparator switching level, and I_{sensor} is the sensor electrode current.

The chosen sawtooth amplitude $V_{sw\text{-}th}$ is 1 V in our case, and the integration capacitance amounts to approximately 140 fF, so that frequencies are obtained between 7 Hz and 700 kHz for the specified sensor current range.

The number of reset pulses is counted with a 22-stage digital counter. Since these counters consume a relatively large portion of the test site area, a design is used which allows to convert the counter circuit into a shift register by a control signal for data readout.

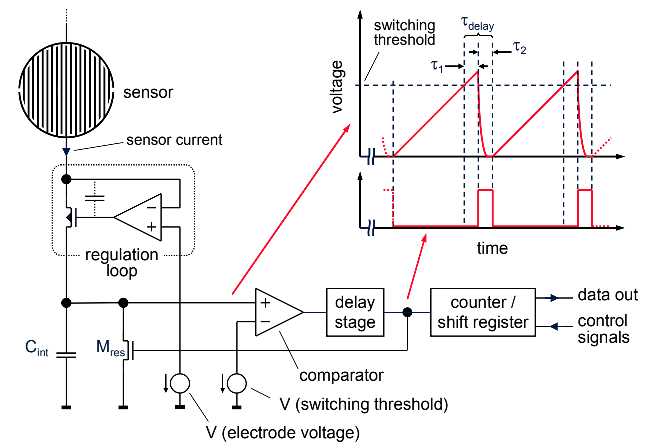


Figure 13: *Circuit principle used for in-sensor site A/D-conversion of the sensor signal based on current-to-frequency conversion. The number of comparator output pulses within a given timeframe is counted by a 22 stage digital counter.*

A more detailed discussion including an evaluation of the excellent accuracy of this approach under consideration of electronic device parameter variations and further circuit design related details is provided in [40].

Dr. Roland Thewes
Phone +49 (0)89 234-41964
E-mail roland.thewes@infineon.com

Neurochip

Neurons on chips

Nerve cells communicate with each other through electrical pulses. However, information processing in biological neuronal networks differs in many aspects from information processing in electronic circuits: Charge carriers on the biological side are ions while microelectronics is based electronic currents. The ability to interface both systems holds the promise of new insights into neurological processes providing the basis for highly specific biosensors in drug screening or man-machine interfaces such as implants or prostheses.

Advantages of CMOS technology

Classical approaches to connect to the electrical signals in neurons such as patch clamping, still suffer from restrictions which prevent long-term multi-site access to neural tissue. However these restrictions can be overcome using large scale integrated, active electronics.
CMOS provides the capability to integrate electronic circuits directly under a planar sensor surface. Active sensor pixels can be designed with high density, which is the basis for a high resolution sensor array enabling electrical imaging of extended neural networks with sub-cellular resolution.

Small pixel design

In order to achieve high-density sensing an extremely small pixel circuit had to be designed which consists of only three transistors as depicted in Fig. 14: One transistor is required for sensing and one for pixel selection. Due to electrical parameter mismatch of the relatively small sensor transistors, a smart calibration technique had to be implemented, which requires a third calibration transistor shortening the gate and drain of the sensor transistors at periodic calibration intervals [41]. The pixel covers an area of 7.8 μm × 7.8 μm including a circular sensor area with 4.5 μm diameter.
Hence, an array of 128 × 128 pixels is integrated within an area of 1 mm × 1 mm. In order to read out the 16384 sensors of the array with a reasonable number of interconnects, column scanning and row multiplexing has been implemented.

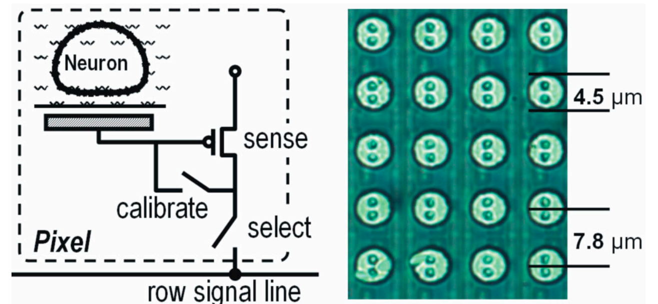


Figure 14: *Pixel circuit (left) consisting of three transistors for sensing, calibration and sensor selection. Cut-out (right) of the sensor array showing 5 x 4 pixels with round sensors.*

Fig. 15 illustrates the increased density of sensor sites between passive metal electrode arrays ($2.5 \times 10^{1} mm^{-2}$) and the CMOS-based sensor array ($1.6 \times 10^{4} mm^{-2}$). The high-density design offers two major benefits:
i) The probability of successful cell-sensor contacts is hardly influenced by biological dynamics. Cells can be placed randomly or may move following the dynamics of network formation without escaping from the sensitive area.
ii) Dense arrays with small pixels enable neurobiological imaging ranging from mapping of ion channel densities of medium-size neurons to activity mapping of large brain slices.

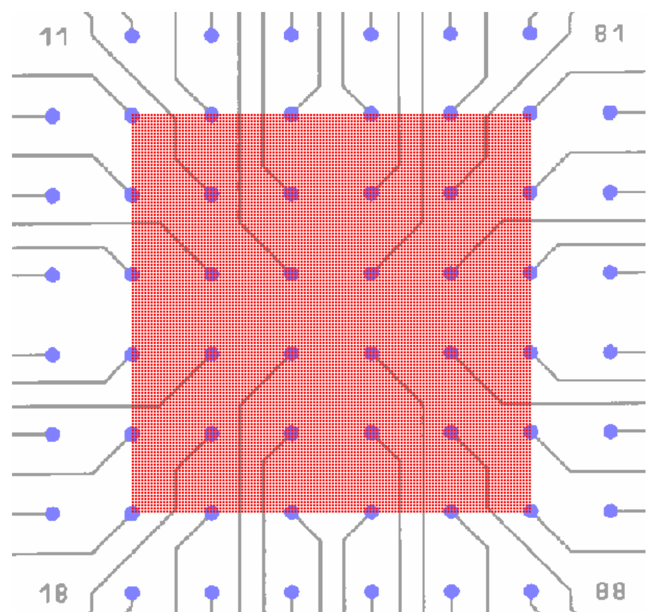


Figure 15: *Visual comparison of sensor density and size between a metal electrode array (blue sensor dots) and the neurochip (red sensor dots).*

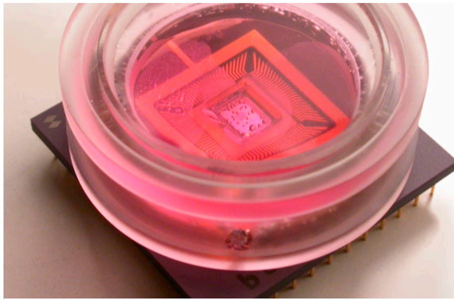


Figure 16: *The package of the neurochip is extended by a perspex culturing chamber containing the nutrition solution for cell culturung. At the open bottom the sensor array is in direct contact with the biological tissue.*

Process challenges

The fabrication of electronic biosensors faces the challenge that, on the one hand, the electrical circuitry has to be passivated against the corrosive influence of the biological environment, which is indispensable for cell culturing. On the other hand, the sensing elements have to be placed at or close to the surface, where the cells are attached.

Classical materials of standard CMOS processes such as aluminum are not biocompatible. Therefore the standard CMOS backend process has to be modified and extended by additional process steps. The metal stack is finished with a Ti/Pt layer and an additional biocompatible dielectric layer of TiO_2/ZiO_2 is deposited on the entire chip surface. This oxide layer prevents diffusion of corrosive electrolyte into the standard CMOS backend stack and ensures a homogeneous sensor surface exhibiting purely capacitive sensing behavior.

Finally a perspex culturing chamber is attached to protect the bonding wires while leaving the active area exposed to the culture medium [42]

High-speed recordings of cells and networks

The neurochip has been developed in close cooperation with the Department of Membrane and Neurophysics at the Max-Planck-Institute of Biochemistry, Martinsried, where experiments with neural tissue are performed.

In order to demonstrate the imaging properties of the neurochip [43], large cells from the pond snail *lymnaea stagnalis* have been selected. These cells are well-known for their good ability to reconstruct neural networks in-vitro.

Before cell culturing, the chips are coated with poly-L-lysine to promote cell adhesion. Nerve cells are dissociated from the snail brain, attached to the chip and cultured over night in a nutrient solution as shown in Fig. 16. During this period the cells adhere tightly to the chip surface where neurites can grow out and reconnect the cells.

In a first example the sensor array of the neurochip is used for mapping the extracellular voltage beneath a single neuron.

A cell on subset of the array is shown in Fig. 17a). The signals of the 32 x 32 pixels in the subset are sampled at 7.9 kHz. The intracellular voltage of the neuron upon stimulation with an impaled pipette is plotted in Fig. 17b) (upper trace) along with the responses of three selected sensor transistors (lower traces). A sensor (71/85) which seems to be beyond the visible soma also records a significant signal. This is due to an extended pan cake-like neurite which an only be seen after fluorescent staining. The

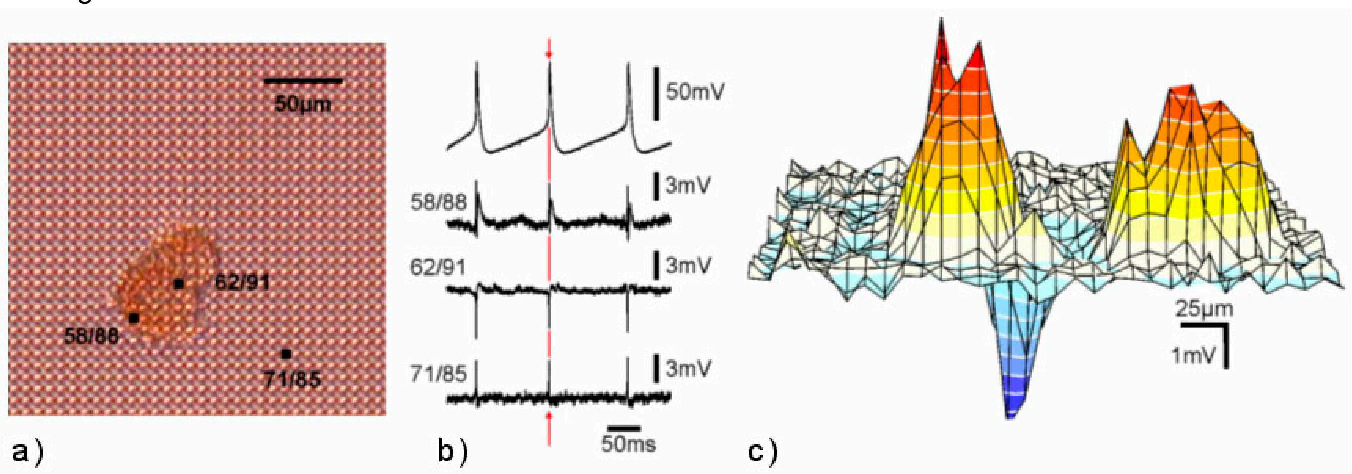
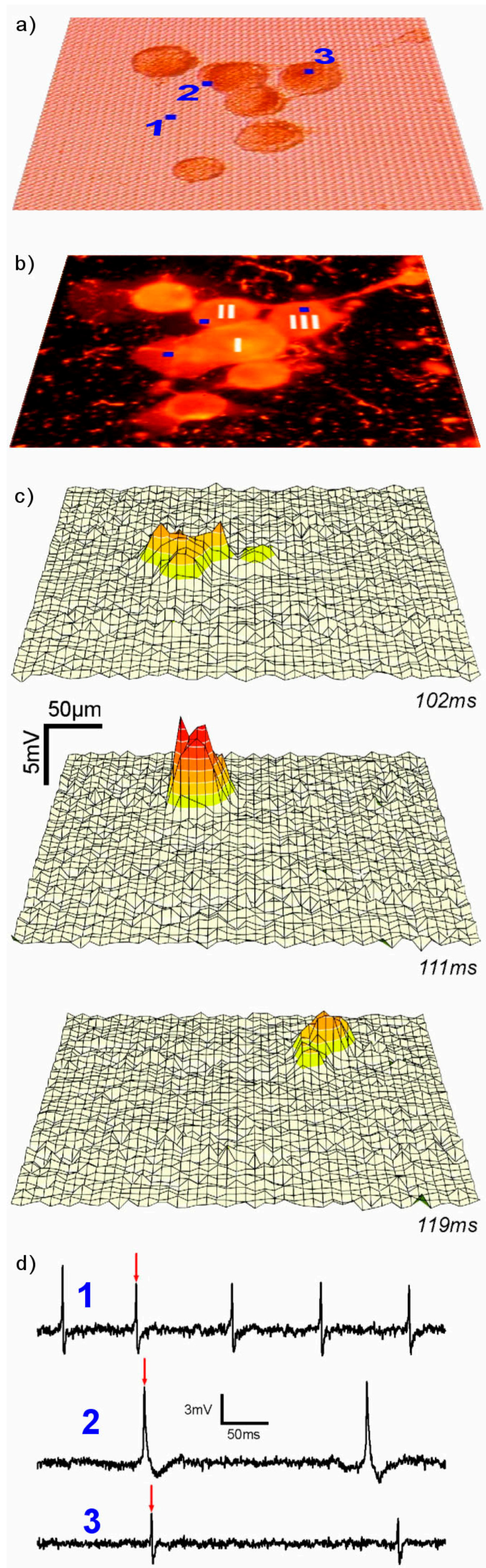


Figure 17: *a) Single cell cultured on a 32 x 32 subset of the sensor array. b) Transients of the intracellular potential (top) and signals at three selected transistors. c) Voltage map at maxima of the recorded peaks (red line in b).*

***Figure 18:** Small network of cultured cells. a) Micrograph from optical microscope. b) Micrograph of the same network after fluorescent staining. c) Three complete voltage maps selected for the maxima of the second action potential in neuron I, of the first action potential in neuron II and of the first action potential in neuron III (arrows in d). In the first frame activity at the grown neurite of neuron I was observed. Notably, only a weak signal is recorded at the cell body. Nine milliseconds later, the recorded activity is localized at the soma of neuron II. An additional eight milliseconds later, electrical excitation is detected at neuron III.*



shape of the three signals differs significantly. Fig. 17c shows a single frame selected at the maxima of the sharp transients. The different shapes of extracellularly recorded signals can be related to inhomogeneous ion channel distribution within the cell membrane giving insight into the current state of the cell.

In a second example the ability of the neurochip to study network dynamics is demonstrated.

On a 48 x 48 subset of the chip six snail neurons are cultured as depicted in Fig. 18a). After staining with the dye DiI the fluorescence micrograph in Fig. 18b) reveals a pancake-like neurite of neuron I. Neurons I and III are impaled with micropipettes. Neurophysiological standard tests reveal that they are connected by electrical synapses. The sensor array records the activity pattern of the small network at a rate of 5300 frames per second after triggering of neuron I by current injection.

The signals of three selected sensors are plotted in Fig. 18d). Transistor 1 beneath neuron I records a primary train of five action potentials. Transistor 2 beneath neuron II detects two action potentials shortly after the second and fourth action potential in neuron I. Neuron III responds shortly after the two action potentials in neuron II with two biphasic signals as recorded by transistor 3.

Both examples illustrate that the neurochip provides a universal sensor platform for the multifold needs from basic research to drug screening.

Dr. Martin Jenkner
Phone +49 (0)89 234-55234
E-mail martin.jenkner@infineon.com

Dr. Roland Thewes
Phone +49 (0)89 234-41964
E-mail roland.thewes@infineon.com

High Frequency Circuits

Silicon-based RF ICs up to 100 GHz: Research Trends and Applications

Introduction

The demand for access to information, anywhere, anyplace, and anytime, will require whole new kinds of information systems. This demand for novel communication systems will translate into innovation in emerging technologies, circuit design methodologies and fabrication techniques. The call for miniaturization, low power consumption, low cost and the move towards higher frequencies for wireless and wireline applications are critical trends influencing the direction of communications system development.

At the core of these approaches, heavy emphasis is placed on finding the right match between circuit techniques and fabrication-process technology. The current cycle sees radio frequency (RF) and microwave integrated circuit engineering having grown rapidly in importance in recent years, stimulated in particular by booming digital mobile communications.

Current indium phosphide (InP) bipolar integrated-circuits support high-performance mixed-signal applications at frequencies up to 200 GHz and beyond [44, 45]. The high cut-off frequencies and high breakdown voltages present a unique combination which addresses some major issues. In the meantime, silicon bipolar and CMOS technologies are not standing still. Silicon germanium (SiGe) has brought substantial improvements in bipolar circuit performance [46, 47, 48, 49, 50]. Recently, CMOS is capturing a significant portion of wireless RF and wireline applications with the promise of lower costs and increased integration scale at highest frequencies [51, 52, 53, 54].

This folder presents some key work done at Infineon Corporate Research, High-Frequency Research Department, which show record benchmark performance. The summarized circuits use a 0.13 µm and 90 nm bulk-CMOS technology and a production-near 200 GHz/275 GHz f_T/fmax SiGe bipolar technology.

Dr. Werner Simbürger
Phone +49 (0)89 234-48432
E-mail werner.simbuerger@infineon.com

A 17 GHz ISM/WLAN RF front-end with only 130 mW power consumption in 0.13 µm CMOS

With growing interest in broadband wireless communication systems and faster and high-performance transceivers at data rates of 100 Mbit/s to 1 Gbit/s and beyond, sub-micron CMOS is particularly attractive for RF and digital baseband processing because of its low power consumption and high integration scale. Emerging short-range applications, such as a high-speed wireless USB 2.0 interface for example, will rely on a low power consumption for mobile systems.

Fig. 1 shows the block diagram of an integrated RF front-end for 17.1-17.3 GHz ISM band application. The high frequency part of the RF transceiver consists of a LNA and mixer [55] and a high-performance PLL [56]. The concept of the dual conversion (Fig. 1) results in a large frequency separation between the RF and LO frequencies and avoids the generation of I/Q

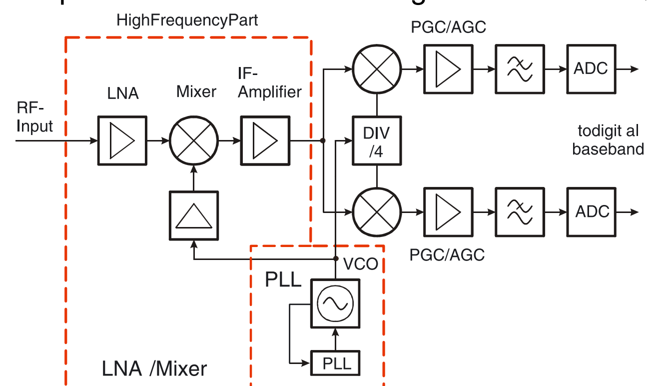
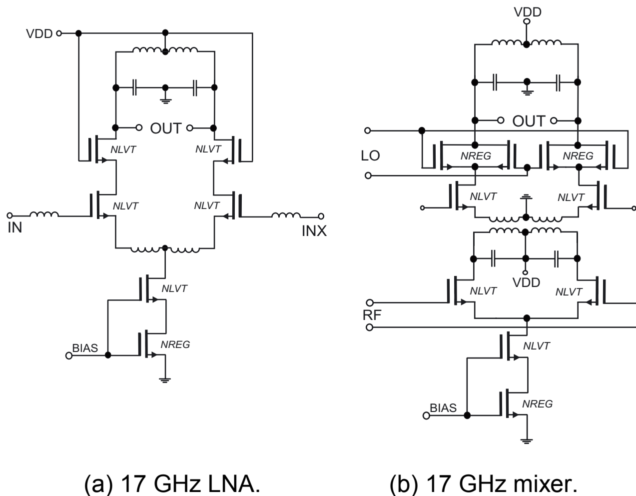


Figure 1: *17 GHz ISM/WLAN RF frontend block diagram [55, 56].*

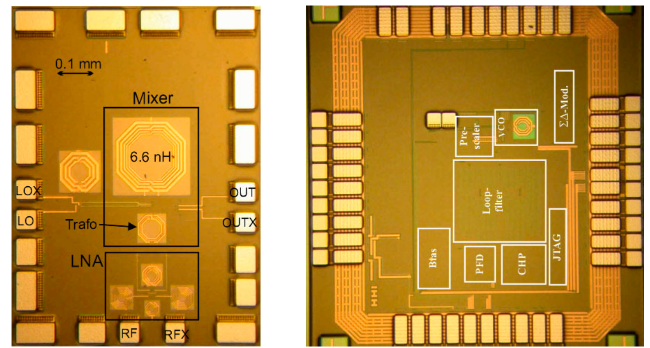
signals at the first LO frequency.
LNA and mixer design is one of the main challenges, since this circuit determines the total gain, noise figure and linearity performance of a receiver. Fig. 2 shows a simplified schematic diagram of the 17 GHz LNA and mixer in 0.13 µm CMOS.



(a) 17 GHz LNA. (b) 17 GHz mixer.

Figure 2: *17 GHz LNA / mixer schematic diagram [55].*

The LNA core in Fig. 2(a) consists of a cascoded, inductively degenerated common source input stage. Inductive degeneration is employed at the common source node of the LNA to achieve a real valued input impedance and low noise figure. The LNA-output is loaded by an integrated LC-tank to increase the gain. Due to the high frequency of 17 GHz all inductors can nicely be integrated without significant area penalty (see chip photograph Fig. 3(a)). A simplified schematic diagram of the mixer is shown in Fig. 2(b). The classical Gilbert-type mixer was preferred to achieve acceptable gain, low noise figure and high linearity. To overcome problems caused by the low supply voltage of 1.5 V in 0.13 µm CMOS, a fully differential integrated transformer was connected between the input transconductance stage and the mixer switching pairs. This topology effectively doubles the voltage headroom available for the circuit design and enables the insertion of cascode transistors to improve the linearity and to control the current in the mixer switching stage. Fig. 3(a) shows the chip photograph of the LNA / mixer. The block diagram of the LNA / mixer is shown in Fig. 1.
In Tab. 1 the measured performance of the 17 GHz LNA / mixer is summarized.
The block diagram of the PLL is shown in Fig. 4.



(a) 17 GHz LNA / mixer. (b) 13 GHz PLL.

Figure 3: *17 GHz LNA mixer and 13 GHz PLL chip photograph [55,56].*

Table 3: 17 GHz LNA / mixer measurement results [55].

Power supply	1.5 V
Total power consumption	70 mW
LNA power consumption	5.2 mW
Mixer power consumption	27 mW
LO-Driver power consumption	12 mW
IF-Amplifier power consumption	25.8 mW
IF frequency	3.4 GHz
LO frequency	13.95 GHz
RF frequency	17.35 GHz
Power gain	34.7 dB
Noise figure SSB	6.6 dB
CP_{1dB} (input)	-39 dBm
IIP3	-34.4 dBm
3 dB bandwidth	200 MHz
Testchip die area	0.88 mm^2
Technology	0.13 µm CMOS

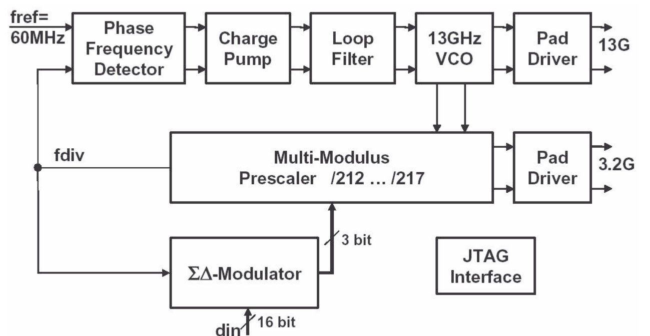


Figure 4: *13 GHz PLL block diagram [56].*

The PLL is completely integrated including VCO, prescaler, phase frequency detector, charge pump, loop filter, biasing, delta-sigma modulator and a JTAG controller [56]. The PLL uses a multi-modulus prescaler with a division rate of 212…217 to allow effective fractional-N synthesis and delta-sigma modulation. Aiming at

a fully integrated high performance 17 GHz transceiver including LNA and output driver, special care was invested to avoid substrate crosstalk, so a differentially tuned LC-VCO was implemented.
In Tab. 2 the performance of the PLL is summarized [56]. The total power consumption of LNA / mixer and PLL is only 130 mW in 0.13 µm CMOS at 17 GHz.

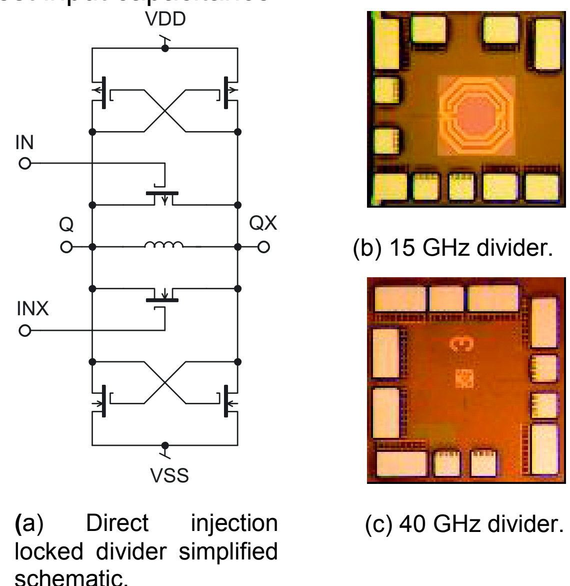
Dr. Marc Tiebout
Phone +49 (0)89 234-53286
E-mail marc.tiebout@infineon.com

Table 2: 13 GHz PLL measurement results [56].

Center frequency	13 GHz
VCO tuning range	8 %
Reference frequency	60 MHz (64 MHz for N=200)
Inband phase noise (@ fvco/4)	-100 dBc/Hz
RMS Phase error (@ fvco/4) (10kHz to 100MHz)	1.6 deg (N=214.5044) 3.0 deg (N=214.992)
Power supply	1.5 V
Total Power consumption VCO Div/4 Prescaler Loop Filter Charge pump Others, incl. Digital	60 mW 5 mW 40 mW 1 mW 5 mW 3 mW 6 mW
Testchip die area	1.8 mm by 1.6 mm
Technology	0.13 µm CMOS

40 GHz, 3 mW low-power injection locked frequency divider in 0.13 µm CMOS

RF Phase locked loops are widely used in wireless and wireline applications as frequency synthesizers or clock sources. Crucial high frequency PLL-components are the voltage controlled oscillator (VCO) and the high frequency dividers. Main concern for VCO-design is low phase noise and low power consumption. Main concern for the frequency divider is lowest power consumption and high frequency capability. High frequency dividers can be realized using CML-logic, using dynamic logic, using a Miller divider or through the injection locking of oscillators. Miller-dividers and CML dividers have been realized up to very high frequencies, unfortunately with high or very high power consumption. Dynamic logic frequency dividers feature a very small power consumption, but the maximum frequency of operation is limited to a few GHz. Injection locked oscillators consume generally less power than CML- or Miller-dividers due to the tuned nature of the circuit. One disadvantage of injection locked oscillators is the limited input bandwidth (or input locking range), which fortunately is not very relevant in LC-VCO based PLL's, as LC-VCO's anyway feature a limited tuning range. The main disadvantage of today's widely used CMOS differential injection locked oscillator topology is found in the large input capacitance and in its small input locking range. A CMOS low power direct injection locking scheme [57] for LC-oscillators is presented in Fig. 5 to divide highest frequency signals with lowest input capacitance.



(a) Direct injection locked divider simplified schematic.

(b) 15 GHz divider.

(c) 40 GHz divider.

Figure 5: *Direct injection locked divider simplified schematic diagram. 15 GHz and 40 GHz injection locked divider chip photograph [57].*

The proposed topology consists of MOS-switches directly coupled to the tank. The concept is verified with two fully integrated injection locked oscillators aiming at different frequencies. The measured frequency locking characteristics and phase noise clearly verifies

the circuit implementation. A CMOS low power injection locked oscillator performs highest frequency division by two consuming only 3 mW from 1.5 V supply voltage. The measured circuit divides 41 GHz by two with a locking range of 1.5 GHz. A second oscillator aiming at 15 GHz features a total locking range of 14.2-17 GHz at a power consumption of 23 mW. The increased locking-range of this divider results in increased power consumption [57].
The measurement results are summarized in Tab. 3.

Dr. Marc Tiebout
Phone +49 (0)89 234-53286
E-mail marc.tiebout@infineon.com

Table 4: Injection locked divider performance [57].

Technology	0.13 µm CMOS	
Supply voltage	1.5 V	
Power Consumption	3 mW	23 mW
Locking Range	40.5 - 42 GHz	14.2 - 17 GHz

A 60-Gb/s 0.7-V 10-mW Monolithic Transformer-Coupled 2:1 Multiplexer in 90nm CMOS

Data multiplexers (MUX) are key blocks in high-speed data communication systems. Current 2:1 MUX already achieve operating speeds of 50 Gb/s in CMOS [58, 53]. However, these MUX circuit concepts suffer from low-supply voltages of future CMOS technologies. In this work a monolithic transformer is used in a high-speed MUX circuit to achieve 60 Gb/s operation at a ultra-low supply voltage of 0.7V [59].
Fig. 6 shows the schematic diagram of the monolithic transformer-coupled MUX circuit. The transformer splits the conventional CML-MUX design into the MUX-Core and the MUX-Clock section and couples the clock signal from the MUX-Clock to the MUX-Core (Fig. 6). There are outstanding advantages due to the on-chip transformer. Because of the missing DC-path between primary and secondary side of the transformer the MUX-core and the MUX-clock section can use the full supply voltage. The effective supply voltage for the MUX 2:1 circuit is doubled. The supply voltage of MUX-core and MUX-clock is connected to the center taps of the monolithic transformer. In this circuit only two transistors are in series using the full supply voltage. The higher drain-source voltage per transistor offer a higher f_t and therefore a higher circuit speed.
Fig. 7 illustrates a 3-dimensional view of the monolithic transformer *X*1 (Outer diameter: 35 µm) The transformer *X*1 is connected as a

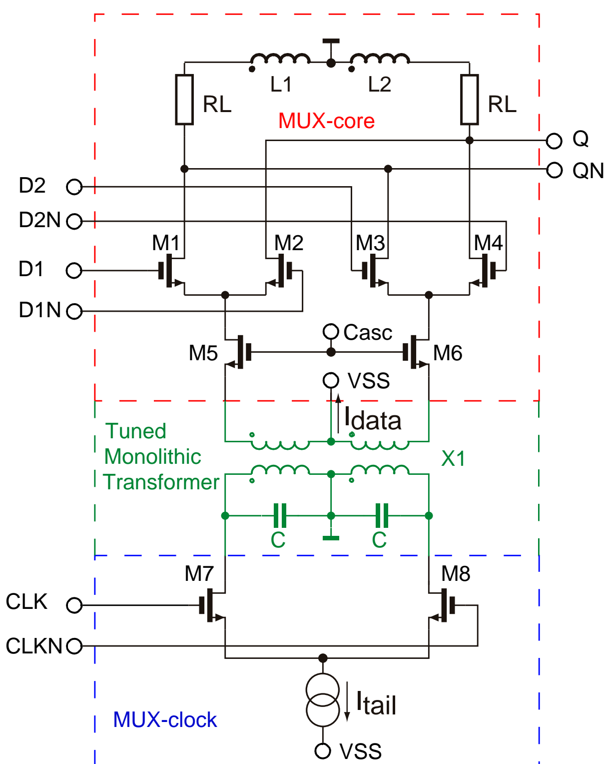


***Figure 6:** 60-Gb/s 0.7-V monolithic transformer-coupled 2:1 multiplexer schematic diagram [59].*

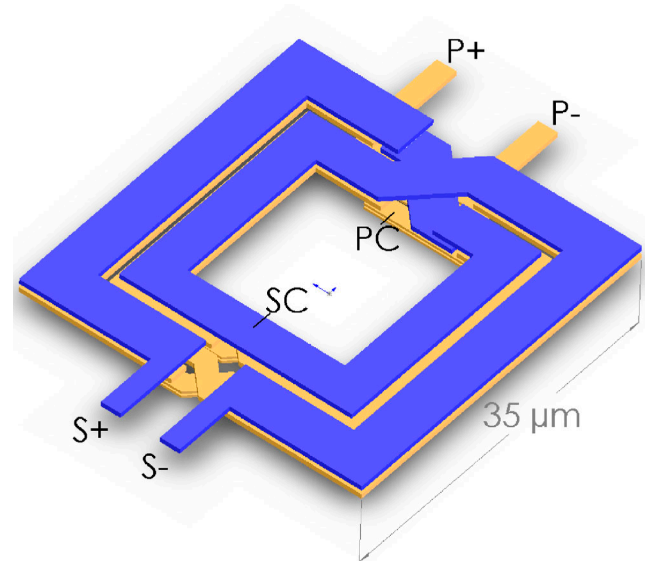
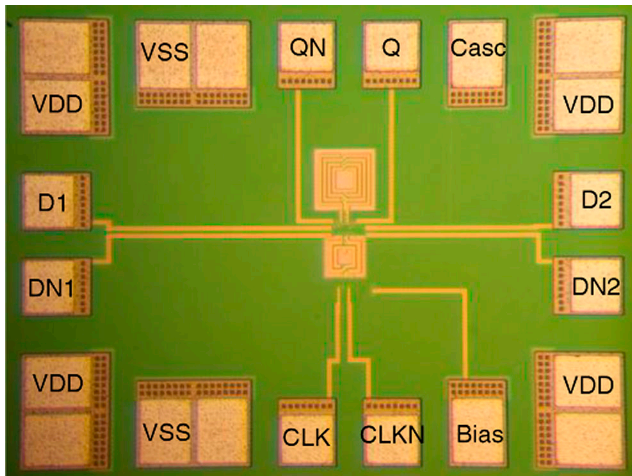
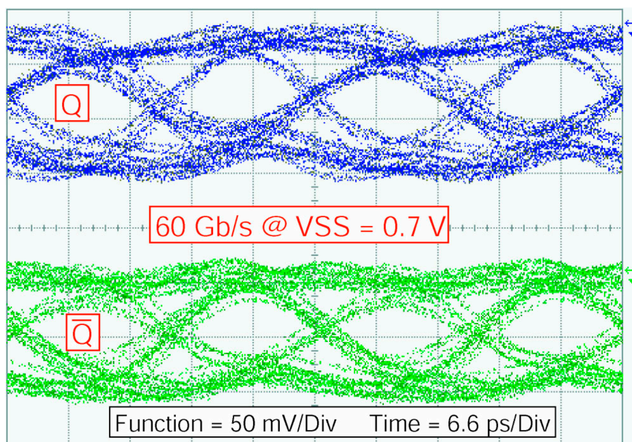


***Figure 7:** 3D-view of monolithic transformer X1 (Outer diameter: 35 µm) [59].*



(a) Chip photograph.



(b) 60-Gb/s measured eye diagram.

***Figure 8:** 60-Gb/s 0.7-V 2:1 MUX in 90 nm CMOS: chip photograph and measured eye diagram [59].*

parallel resonant device. The MOS capacitors *C* are connected in parallel to the primary windings of the transformer. The resonant tuning increases the current transfer ratio of the transformer. The cascode transistors *M*5 and *M*6 provide isolation between the data-path transistors *M*1-*M*4 and the transformer's parasitic capacitances. The cascode also sets the bias current for the MUX-core. The data-path transistors *M*1-*M*4 switch the current to the load resistor. Shunt peaking is used to enhance the bandwidth of the MUX [60]. The shunt peaking inductor is realized as a differential inductor. The inductance value of *L*1 and *L*2 is 0.36 nH. The tail current *Itail* is set to 8 mA. A resistive divider sets the DC level of the sinusoidal clock signal to VSS/2 and works as input matching network for the clock signal.
For measurement the 2:1 MUX IC is bonded on a ceramic microwave substrate. The multiplexer is tested with two pseudo-random bit sequences (PRBS of 2^{11}-1). The input voltage swing is 2 x 350 mV_{pp}. The sinusoidal clock signal has a voltage swing of 2 x 400 mV_{pp}. Fig. 8(b) shows the measured eye diagram of the single-ended outputs at a data rate of 60 Gb/s. Tab. 4 shows the performance summary of the MUX.

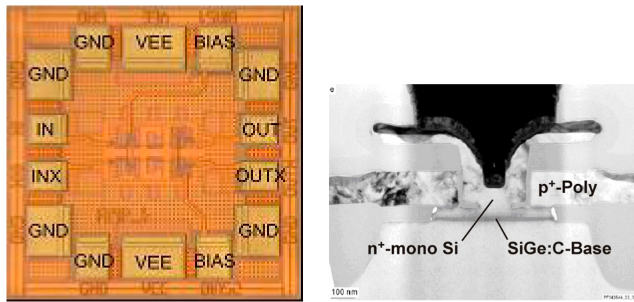
Table 5: 50 Gb/s 2:1 MUX measurement results [58].

Power supply	0.7 V
Total power consumption	10 mW
Maximum data rate	60 Gb/s
Output voltage swing (50 Ω)	2×50 mV_{pp}
Testchip die area	0.63 mm by 0.47 mm
Technology	90nm CMOS

Dr. Daniel Kehrer
Phone +49 (0)89 234-48490
E-mail daniel.kehrer@infineon.com

A 100 Gbit/s amplifier in SiGe bipolar technology

A broadband amplifier with 16 dB gain and a 3-dB bandwidth of 62 GHz has been realized in a 200 GHz f_T, 275 GHz f_{max} SiGe bipolar technology [61, 62]. Broadband amplifiers are very important building blocks for a large variety of applications, including wireless transceivers, mm-wave applications and optical communication systems. In general, they are based on a lumped [63, 64, 65] or on a distributed concept [66, 67, 63].
The circuit diagram of the broadband amplifier based on lumped elements realized in this work is shown in Fig. 9. The amplifier is based on a fully differential design and consists of two stages. 50 Ω on-chip resistors are provided at the input and the output for broadband matching. In addition, emitter degeneration and low load resistors are used for increasing the 3-dB bandwidth at a well-defined gain. Carefully adjusted transistor sizes and currents enable a flat transfer function and a high bandwidth. The differential amplifier of the second stage is implemented as cascode configuration in order to prohibit avalanche breakdown of the output



(a) Amplifier chip photograph. (b) SiGe BJT TEM cross section.

Figure 10: *Chip photograph of the 62 GHz, 16 dB gain broadband amplifier in SiGe (chip size: 550 µm × 550 µm) [61] and TEM cross section of the emitter-base complex of a SiGe transistor with effective emitter width of 0.14 µm [62].*

transistors. The cascode stage additionally minimizes the Miller effect, thereby bandwidth is increased.

The chip photograph of the amplifier is shown in Fig. 10(a). The amplifier is fabricated in a preproduction SiGe bipolar technology [62]. The transistors have a double-polysilicon self-aligned emitter-base configuration with a minimum effective emitter width of 0.14 µm. A TEM cross section of the emitter-base complex is given in Fig. 10(b). The SiGe:C base of the transistors has been integrated by selective epitaxial growth. The emitter contact exhibits a monocrystalline structure. The transistors manufactured in this technology offer a transit frequency f_T of 200 GHz, a maximum oscillation frequency f_{max} of 275 GHz and a ring oscillator gate delay of 3.5 ps. Current density for maximum f_T and f_{max} is at about 8 mA/µm^2. The collector-emitter breakdown voltage BV_{CE0} is 1.7 V. The technology provides four copper metallization layers, two different types of polysilicon resistors, a TaN thin film resistor and a MIM capacitor.

The single-ended low-frequency gain is 10 dB and the 3-dB bandwidth is 62 GHz. The differential gain is 16 dB. The current consumption is 155 mA at a supply voltage of -5 V. Degradation of S_{22} at about 50 GHz can be observed. In the case of a single-ended excitation together with an inductance in the supply path this behavior can be verified by simulations. In differential operation such an inductance will have no effect.

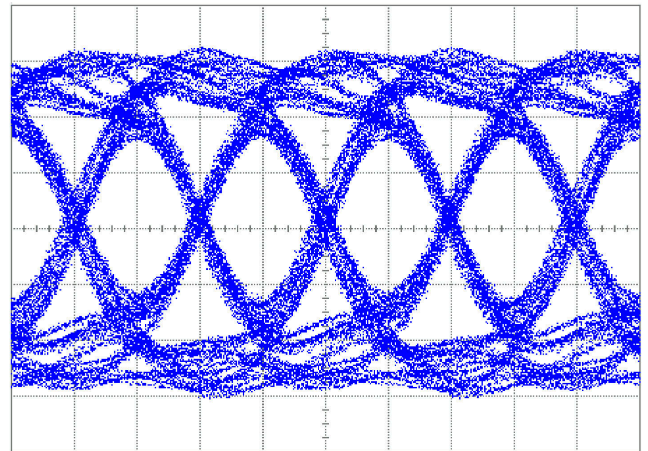


Figure 11: *100 Gb/s (250 mV/div, 5 ps/div) [61].*

In Fig. 11 the measured output eye diagram for a 100 Gbit/s excitation signal is shown. A high-performance PRBS-generator chip [49] and the broadband amplifier chip have been mounted closely on a substrate. Short bond wires connect the outputs of the PRBS-generator and the amplifier inputs. The clear output eye diagram at a data rate of 100 Gbit/s demonstrates the feasibility for high-speed communications. Tab. 5 shows the performance summary.

Table 6: Broadband amplifier measurement results [61].

SiGe bipolar technology, min. eff. emitter width, ring osc. gate delay	200/275 GHz f_T/f_{max} 0.14 µm 3.5 ps
Bandwidth (3 dB)	62 GHz
Differential gain	16 dB
CP_{1dB} (input)	-9.5 dBm
IIP3	+2.1 dBm
Supply voltage	-5.0 V
Supply current	155 mA
Chip size	550 µm × 550 µm

Werner Perndl
Phone +49 (0)89 234-45102
E-mail werner.perndl@infineon.com

A 65 GHz - 95 GHz double-balanced mixer for automotive radar front-ends in SiGe bipolar technology

An active mixer for down-conversion with a conversion gain of more than 24 dB and single-sideband (SSB) noise figure of less than 14 dB in the frequency range from 76 GHz to 81 GHz has been realized [68]. The gain is >22 dB from 65 GHz up to 95 GHz with slightly decreased noise performance.
A simplified circuit diagram of the mixer is shown in Fig. 12. The mixer consists of a mixer core, an LO buffer, a balun at the RF input and an IF buffer. The mixer core is based on the Gilbert-mixer. The mixer has a double-balanced structure and utilizes differential LO and RF signals. Transistor sizes and bias currents are optimized in order to obtain a good compromise between gain, linearity and low noise figure. The size of the switching transistors is designed at the current density for maximum f_T, whereas the RF transistors are designed for minimum noise contribution. The differential signals required for LO and RF inputs of the mixer core are generated by the LO buffer and a LC balun, respectively. The LO buffer consists of a differential amplifier which provides a differential output signal from the single-ended input.

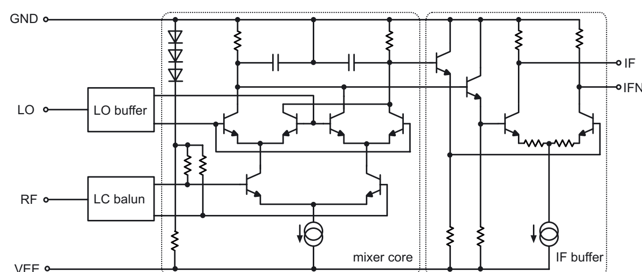
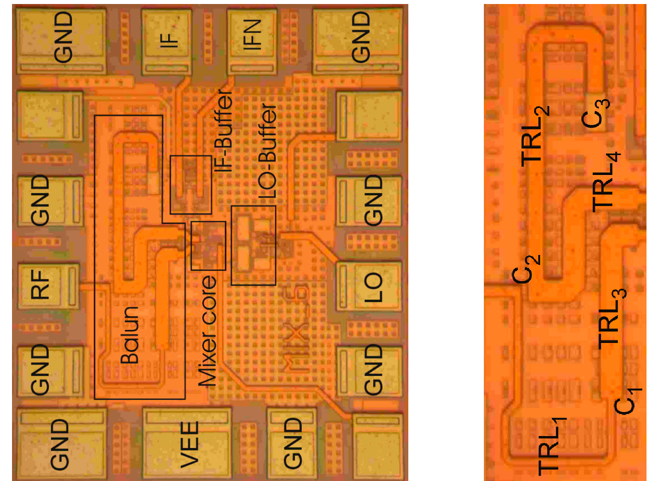


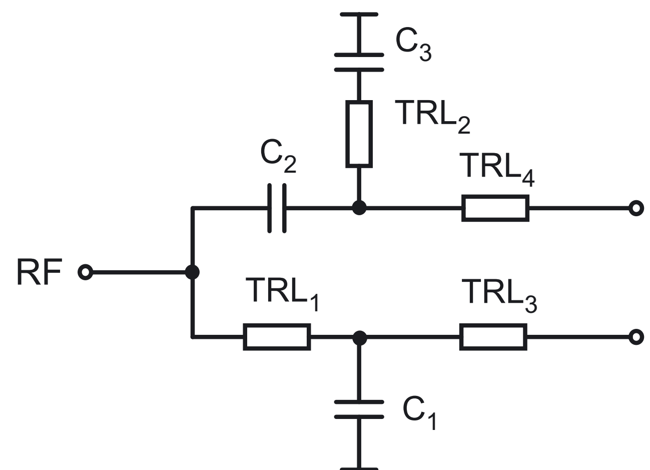
Figure 12: *Simplified circuit diagram of the mixer (GND = 0 V, VEE = -5 V) [68].*

Fig. 13(a) shows the chip photograph of the mixer. Building blocks and important pads are indicated in the photograph. The LC balun (Fig. 13(b)) is placed directly at the RF input, followed by the mixer core. The LC balun consisting of the transmission lines TRL_1 and TRL_2 and the MIM-capacitors C_1 and C_2 (Fig. 13(c)). This balun converts the unbalanced RF signal to a balanced signal and provides an impedance transformation for 50 Ω matching at the RF input. Capacitor C_3 is required to achieve an RF ground at TRL_2. The LC balun was



(a) Mixer chip photograph.

(b) Detailed view of the LC balun.



(c) Schematic diagram of the LC balun.

Figure 13: *Chip photograph of the mixer (chip size: 550 μm × 450 μm), detailed view of the LC balun and schematic diagram of the LC balun [68].*

designed based on the calculation of a lumped element balun [69]. Then the inductances were substituted with transmission line TRL_1 and TRL_2 [70]. Further optimization was done using an EM-field simulator.
The mixer is fabricated in a SiGe bipolar technology which is based on the process technology presented in [71]. The transistors have a double-polysilicon self-aligned emitter-base configuration with an effective emitter width of 0.18 μm. The SiGe:C base of the transistors has been integrated by selective epitaxial growth

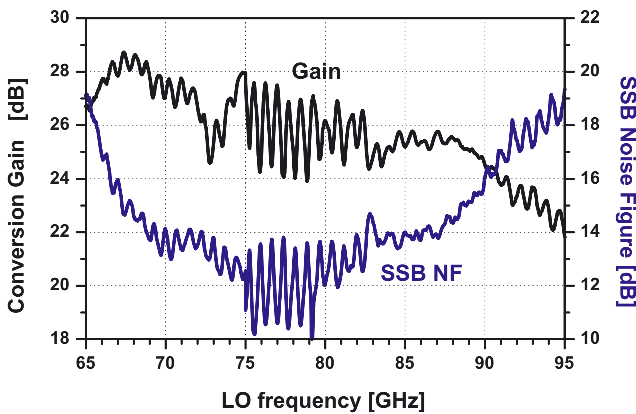


Figure 14: *Measured conversion gain and SSB noise figure versus LO frequency. IF frequency is 500 MHz, LO power is 2 dBm [68].*

and the transistors exhibit a monocrystalline emitter contact. The transistors manufactured in this technology offer a transit frequency f_T and a maximum oscillation frequency f_{max} of more than 200 GHz and a ring-oscillator gate delay of 3.7 ps. The technology provides four copper metallization layers, two different types of polysilicon resistors and a TaN thin film resistor.
In Fig. 14 the measured conversion gain and SSB noise figure versus LO frequency of the mixer at a constant IF frequency of 500 MHz are shown. The LO input power is set to 2 dBm at the center frequency. The measured conversion gain is higher than 24 dB and the SSB noise figure is lower than 14 dB at the frequency range from 72.3 GHz to 82.5 GHz. The mismatch of the mixer RF input and the noise source output result in a ripple seen in the measurement plot. The V-band noise source (frequencies below 75 GHz) exhibits a better match than the W-band noise source (frequencies above 75 GHz). Tab. 6 shows the performance summary of the mixer.

Table 7: Mixer performance summary [68].

SiGe bipolar technology, min. eff. emitter width, ring osc. gate delay	>200 GHz f_T, f_{max} 0.18 µm 3.7 ps
22.4cmConversion gain	>24 dB (65.0 - 90.8 GHz) >22 dB (65.0 - 94.9 GHz)
22.4cmSSB noise figure	<14 dB (72.3 - 82.5 GHz) <16 dB (66.5 - 90.0 GHz)
CP_{1dB} (input)	-30 dBm
Supply voltage	-5 V
Supply current	60 mA
Chip size	550 µm × 450 µm

Werner Perndl
Phone +49 (0)89 234-45102
E-mail werner.perndl@infineon.com

100-Gb/s 2^7-1 and 54-Gb/s 2^{11}-1 PRBS Generators in SiGe Bipolar Technology

Pseudo-random bit sequence (PRBS) generators are widely used to provide test signals for circuits such as multiplexers, demultiplexers and amplifiers. The maximum data rate provided by commercial PRBS generators is in many cases insufficient to test high-speed circuits manufactured in advanced CMOS and SiGe bipolar technologies. Therefore we have designed two PRBS generator ICs to simplify testing of these high-speed CMOS and SiGe ICs.
PRBS generators are based on linear feedback shift registers. The number of shift register stages N determines the length of the resulting pseudo-random sequence, which is 2^N-1 bits. Typical values for N range from 7 to 31. The large number of flip-flops in the shift register, which have to be clocked synchronously, poses the main challenge in the design of high-speed PRBS generators. By making use of special properties of the pseudo-random sequences it is possible to clock the shift register at a fraction

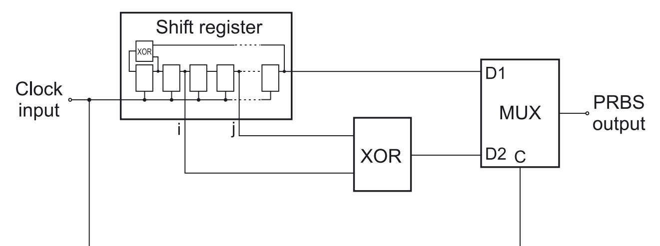


Figure 15: *PRBS generator using a half-rate shift register clock.*

(e.g. one half [72, 73] or one quarter [74]) of the output data rate. The output signal is then generated by using additional XOR gates and multiplexers (Fig. 15).
We have developed two PRBS generator ICs. One circuit is designed for high output data rates in the 100 Gb/s range and consists of a seven-

stage shift register operating at one half of the output data rate. The second circuit evaluates the possibility of a full-rate design for 40 Gb/s applications, combined with a longer pseudo-random sequence. It contains an eleven-stage shift register operating at the full clock rate. It does not require a multiplexer at its output and is therefore not susceptible to duty-cycle distortion. The PRBS generator ICs contain additional circuitry to provide a trigger output. Depending on the level at the trigger select input this output provides either a trigger signal for the display of eye diagrams or a trigger synchronous to the

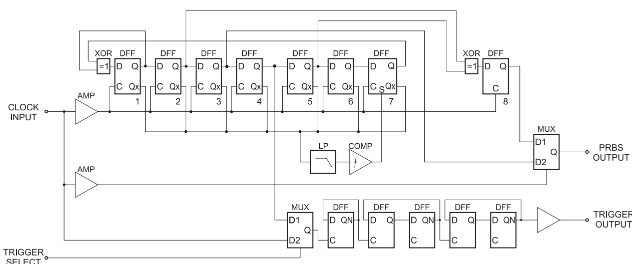


Figure 16: *Block diagram of the 2^7-1 PRBS generator.*

output data sequence to display the bit pattern. This pattern trigger is generated by applying the output data to a frequency divider with a divide ratio of 2^{N-2} [72].

Fig. 16 shows the block diagram of the 2^7-1 PRBS generator. The shift register contains seven master-slave flip-flops. An eighth flip-flop is used for re-timing between the XOR gate and the multiplexer. The multiplexer provides the output signal without any additional buffer or amplifier.

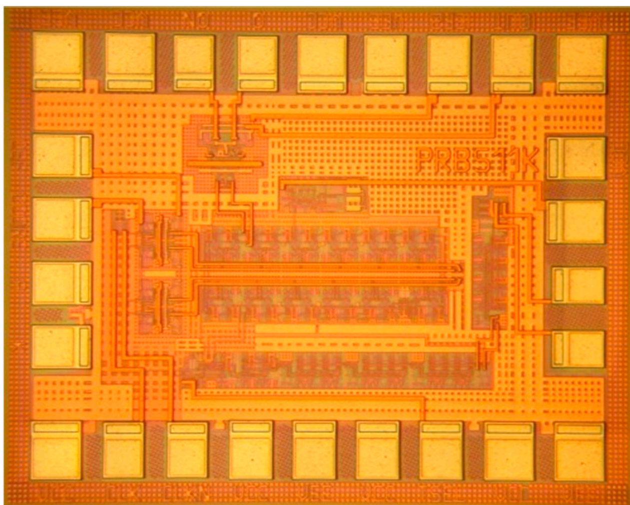
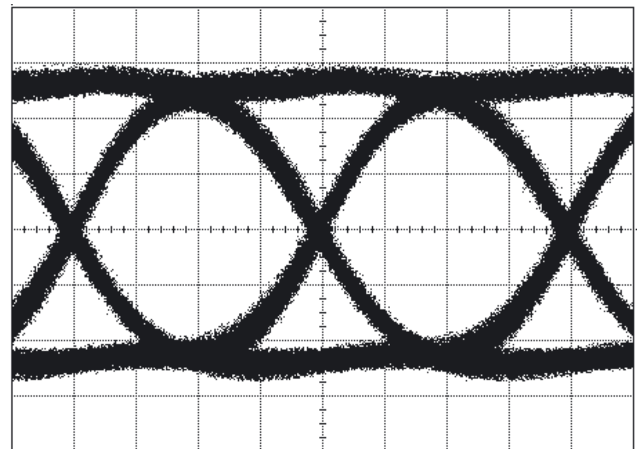


Figure 17: *Chip photograph of the 2^{11}-1 PRBS generator [75].*

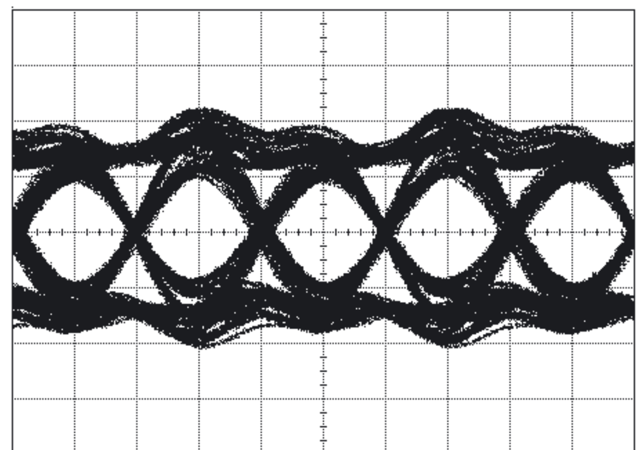
A five-stage frequency divider generates the trigger output signal. Depending on the level at the trigger select input the divider input is either connected to the clock input to provide a trigger output for eye diagrams, or to one of the shift register stages to provide a pattern trigger.

The 2^{11}-1 PRBS generator contains eleven shift register stages which operate at the full clock rate. Therefore no multiplexer is required at the output and a two-stage buffer is used to provide the output signal. The trigger circuit (consisting of nine divider stages) and the auto-start circuit are implemented similar to the 2^7-1 PRBS generator. The chip size is only 0.9 x 0.7 mm^2 (Fig. 17).

First measurements of the PRBS generator ICs were done on wafer using 40 GHz GSSG



(a) 2^{11}-1 PRBS: 54 Gb/s output signal (4.6 ps/div, 150 mV/div)



(b) 2^7-1 PRBS: 100 Gb/s output signal (5 ps/div, 100 mV/div)

Figure 18: *Measured eye diagrams of 2^{11}-1 and 2^7-1 PRBS generators [75].*

probes. Both circuits operate with a supply voltage of 5 V. The 2^{11}-1 PRBS generator consumes 380 mA and operates up to 54 Gb/s with a differential output voltage swing larger than 600 mVpp (Fig. 18(a)).
The 2^{7}-1 PRBS generator consumes 300 mA and operates up to 100 Gb/s (Fig. 18(b)). The eye opening at this data rate is degraded by the limited bandwidth of the measurement setup.

Dr. Herbert Knapp
Phone +49 (0)89 234-52018
E-mail herbert.knapp@infineon.com

Summary

Silicon-based RF ICs have been realized to demonstrate wireline, wireless and sensor applications up to 100 GHz. Finding the right match between circuit techniques and process technology is a major issue to push the circuit performance to the limits. Further advances in process technologies and circuit design will result in continuing the upward shift of the frequency limits in silicon.

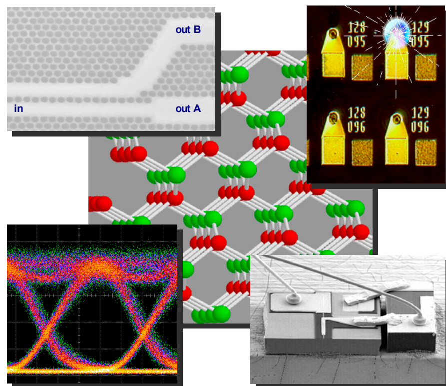
Acknowledgement

The authors would like to thank all Infineon CMOS and SiGe teams which are responsible for process technology development and fabrication.

Photonics

Introduction

The field of Photonics is based on the utilisation of the unique properties of photons: Photons carry energy at the speed of light, do not interact with each other and are not susceptible to ambient electromagnetic fields. Photonic applications range from data transmission in fiber optical networks to displays, solar cells and laser-based material processing.
Infineon has been involved in photonic technology in the field of high-bandwidth optical data transmission systems including the manufacture of the corresponding HF electronics.
The carve-out of the business unit Fiber Optics changes this situation and consequently affects the future focus of our department.
The department of Photonics (CPR PH) has concentrated its work on key optoelectronic components for future high-bandwidth communication systems.
We address the design, HF modelling as well as the realisation of high-bandwidth components and the verification of their performance. Moreover, we carry out application-oriented materials and technology exploration.



Projects

1) Long-wavelength GaAs-based lasers
One focus of our department lies on novel heterostructures for GaAs-based surface-emitting lasers (VCSELs), which are capable of emitting beyond 1.3 µm. Such devices are suited for data rates up to 10 Gbit/s.
The field of long-wavelength lasers on GaAs is entirely material-driven. Therefore we operate our own technology lab with facilities for growth and characterisation of novel III-V materials. Its most prominent result was the first demonstration of monolithic 1.3 µm VCSELs. After transferring this technology to the business unit, we continued our work to obtain the longest wavelengths demonstrated so far (up to 1.59 µm) which may open up high-volume applications such as fiber-to-the-home systems.
Due to the shift in Infineon's strategy, this activity has been terminated and the material lab's activity is redirected into the field of nanoelectronics.
2) Laser-Modulator Integration
Another focus lies on novel devices for data transmission beyond 40 Gbit/s. At these data-rates, direct modulation of lasers is no longer possible. Our work is based on a proprietary approach for a monolithic integration of a laser with an electro-absorption modulator. The project is closely aligned with the development of high-speed SiGe electronics in the department of High Frequency Devices (CPR HF). Recently, we have demonstrated one of the fastest laser-modulator chips which achieves a data rate up to 40 Gbit/s with high extinction ratio at a voltage swing that is compatible with SiGe drivers.
In the course of this work, we have developed design tools for the complete optoelectronic and electrical HF characteristics. For processing of devices we closely collaborate with other groups, both at Infineon Fiber Optics and externally.
Within a year, this activity will be brought to an end with results transferred to Infineon Fiber Optics.
3) Photonic Crystal Structures
In close collaboration with universities and research institutes, we conduct exploratory research on photonic crystal structures. The strong guiding of light allows for integrated optical resonators, miniaturisation of passive optical components and integrated optical chips. Owing to rapid technological progress, novel tuneable lasers and the most compact chromatic dispersion compensators have already been realised.
Moreover, a simulation tool developed within the consortium has shown superior performance for mask simulation at MP. This tool will be further tested with respect to its suitability for field simulation in high-frequency applications.

Dr. Henning Riechert
Phone +49 (0)89 234-45230
E-mail henning.riechert@infineon.com

Long-Wavelength GaAs-based Lasers: Demonstration of Low Thresholds Beyond 1500 nm

Introduction

Vertical cavity surface-emitting lasers (VCSELs) are most suitable as low-cost light sources for optical data communication over metro area distances. For the realization of such devices, GaAs-based technology is ideal. However, in this material system it has long been a major problem to achieve band gaps small enough to allow light emission at 1.3 µm. Through the use of InGaAsN as a novel active laser material, our group has pioneered the realization of 1.3 µm VCSELs, and we have subsequently transferred this technology to production at Infineon Fiber Optics. To open up a wider range of applications, it is desirable to extend the emission wavelength over the whole span of system-relevant wavelengths, i.e. up to 1.55 µm. It would then be conceivable to employ low-cost VCSELs in the high-volume market of fiber-to-the-home applications for all three standard wavelengths.

The reduction of the band gap energy in InGaAsN is due to the incorporation of nitrogen. However, this is accompanied by a significant degradation of material quality. That is why for a long time it was questioned if devices with suitable overall performance could be realized for wavelengths beyond 1.3 µm. Therefore, the challenge to reach longer emission wavelengths lies in increasing the N content without compromising material quality.

We have undertaken a systematic investigation of this question, using simple edge-emitting lasers as a test vehicle to assess material quality. Optimizing the growth and annealing conditions resulted in record-low threshold current densities at laser wavelengths up to 1590 nm.

Material issues

A detailed analysis of our best 1.3 µm-lasers reveals that more than 50% of the threshold current is consumed by defect-related recombination (Collaboration with University of Surrey).Thus, the performance of InGaAsN-lasers could be enhanced significantly, if this recombination path were suppressed. Therefore, we have aimed considerable research efforts at improving the material quality of InGaAsN.

Samples were grown on GaAs substrates in a solid source molecular beam epitaxy (MBE) system with a commercial RF plasma source for the incorporation of nitrogen. Particular care was directed at precisely and reproducibly controlling the operation of the plasma source as well as the low growth temperature of the InGaAsN quantum well (QW) region.

In general, material quality was optimized by maximizing the photoluminescence (PL) intensity measured at room temperature. The data in Fig. 1 show that there is a good correlation between PL intensity and laser threshold current density, justifying this approach. Initial experiments were carried out with simple test structures instead of lasers to speed up progress.

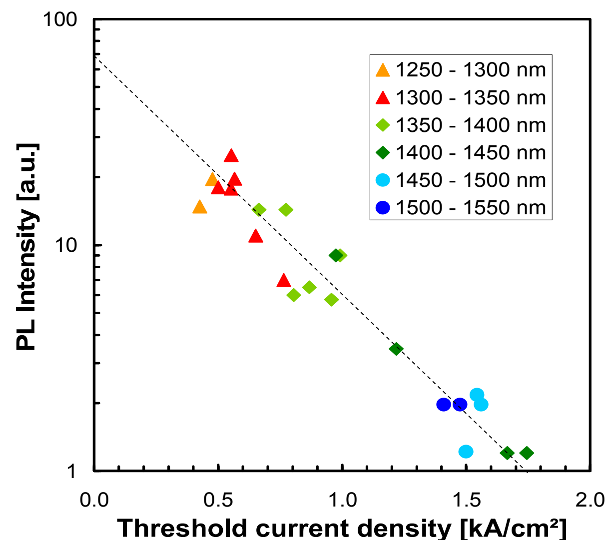


Figure 2: *Correlation between PL intensity and threshold current density of InGaAsN single QW lasers with different compositions of the active region.*

In order to achieve a quality suitable for lasers, InGaAsN has to be thermally annealed after growth. This second step makes the optimization procedure very complex, as illustrated in Fig. 2. The PL intensity of the “as grown” material varies significantly with growth temperature, which is the most important growth parameter. However, upon standard-annealing

(2h, 680°C) the maximum of the curve shifts to much higher growth temperatures. The PL intensity of InGaAsN grown at around 400°C is actually reduced. A variation of the annealing conditions in a wide range resulted in the dashed curve that shows the highest PL intensities that were obtained for each growth temperature. The optimum annealing conditions are different for each growth temperature. Thus, growth and annealing conditions cannot be optimized independently.

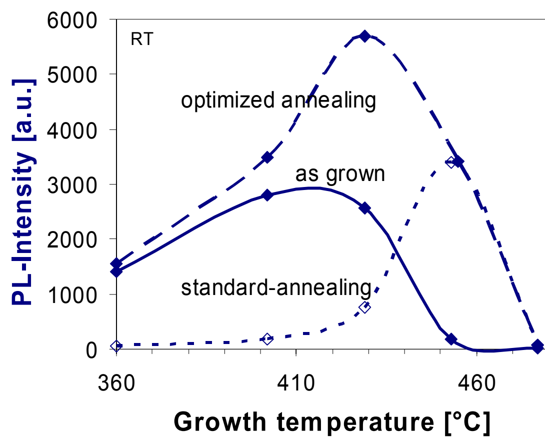


Figure 3: *PL intensities of 6.5 nm thick $In_{0.37}Ga_{0.63}As_{0.983}N_{0.017}$ single QW samples measured directly after growth or after different subsequent annealing treatments.*

Material optimization is complicated further by two additional factors. First, other growth parameters like, most eminently, the arsenic flux influence both the "as grown" PL intensity as well as the effect of different annealing treatments. Second, annealing changes not only the PL intensity but can reduce the wavelength by up to 100 nm. Again, this blueshift depends both on the growth and the annealing conditions. As an experimental screening of all conceivable combinations of growth and annealing parameters is nearly impossible, it is essential to obtain a scientific understanding of the microscopic processes that underlie both preparation steps.

For studies aimed at elucidating the peculiarities of InGaAsN as a material, our own experiments are often complemented by collaborations with university groups. For example, the spatial distribution of In and N within a QW can be extracted from transmission electron microscopy (TEM) images, as depicted in Fig. 3. Since InGaAsN is a quaternary compound, the determination of the local composition requires a very elaborative analysis of TEM images taken under different diffraction conditions. The diagram in Fig. 3 shows that in the "as grown"-material (red line) the In concentration varies significantly along the QW (i.e. perpendicular to the growth direction). Further studies yielded that such compositional fluctuations can be suppressed by lowering the growth temperature. After annealing (black line), the profile of the In-concentration does not have very eminent maxima and minima any more. Hence, annealing causes a homogenization of the composition in the QW.

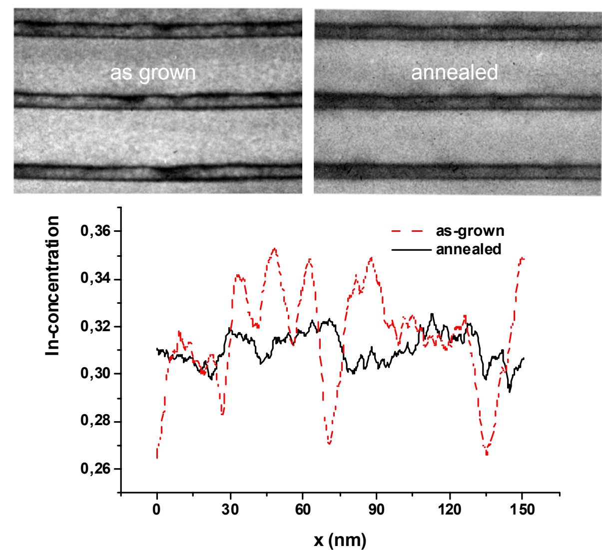


Figure 4: *Transmission electron micrographs of 6.2 nm thick $In_{0.36}Ga_{0.74}As_{0.981}N_{0.019}$ multiple QWs before and after annealing; and profile of the In concentration along the QW.*

Lasers

The ultimate test for the material quality is the performance of edge-emitting lasers. Fig. 4 displays the threshold current density j_{th} as a function of the laser wavelength. Literature values and old data from our group are included for comparison. The diagram comprises three series of experiments. At first (red spheres), the In content of 6.5 nm thick InGaAsN SQWs was kept fixed at 34%, while the N concentration was varied from 2.5% (λ=1280 nm) to 4% (λ=1430 nm). While the increase in j_{th} is only moderate up to 1380 nm (factor 2 per 100 nm), it becomes dramatic above this value (factor 2 per 50 nm).

For the second series of experiments depicted in Fig. 4 (green spheres), the same structure as mentioned above was used with N contents around 4% but with an increase of the In content

to 40% and of the quantum well thickness to 7.5 nm. In addition to the changes in composition and thickness, the annealing conditions were optimized. This step made it possible to keep the threshold current density constant for a wavelength range of more than 50 nm. The longest lasing wavelength that was achieved this way is 1510 nm. For 800 µm long devices the average value is j_{th} = 1.4 kA/cm². The lowest threshold current density for 1200 µm long devices is 780 A/cm² at 25°C, clearly setting a new record for GaAs-based lasers with any kind of active material in this wavelength region.

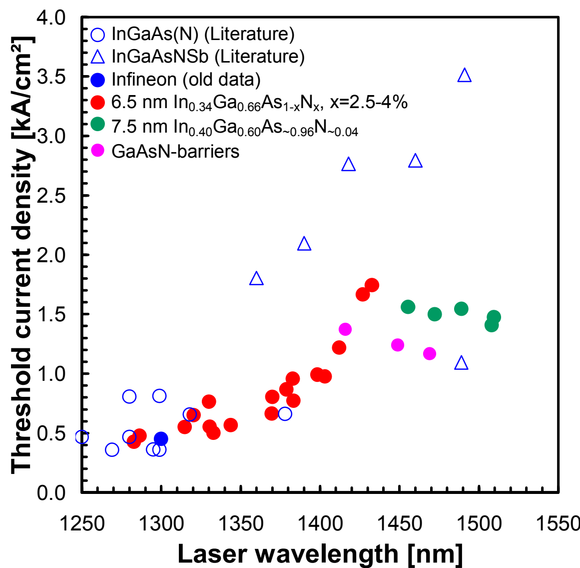


Figure 4: *Threshold current densities of 800 µm long SQW broad area lasers measured at room temperature under pulsed conditions.*

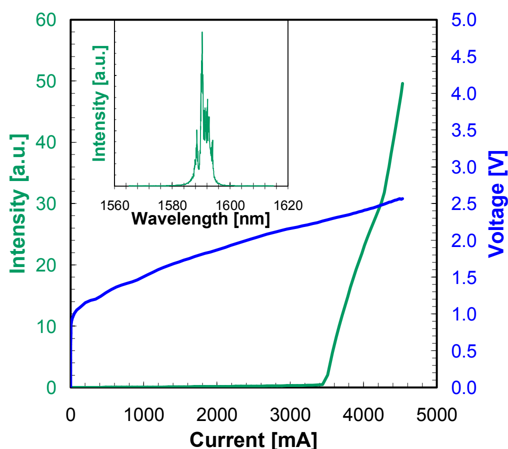


Figure 5: *Light-current and voltage-current curves for a 1200 µm long $In_{0.40}Ga_{0.60}As_{0.95}N_{0.05}$ SQW broad area laser measured at 15°C. Inset: Laser spectrum.*

The main change for the third series (magenta spheres) was the use of GaAsN- instead of GaAs-barriers. This change in design rather than in material quality leads to a further reduction of the threshold current density. These data show that an additional optimization of the laser design holds the prospect of still better device performance.

Pursuing the goal of even longer wavelengths, we increased the N content to 5% without any new optimization of the preparation conditions. The corresponding laser data are shown in Fig. 5. $In_{0.40}Ga_{0.60}As_{0.95}N_{0.05}$ as active material resulted in lasing at 1590 nm with a threshold current density of 2.9 kA/cm². This is the longest wavelength of a GaAs based laser that has ever been reported, not taking into account quantum cascade lasers that are based on a completely different principle.

Conclusions

We have shown that InGaAsN is a suitable active material for GaAs-based lasers with emission wavelengths of 1.5 µm. Growth and annealing conditions have to be optimized dependently on each other. At a wavelength of 1510 nm, SQW lasers with a threshold current density of 780 A/cm^2 have been achieved. Also, lasing has been demonstrated at 1590 nm. These results suggest that 1.5 µm-VCSELs on the basis of InGaAsN QWs are feasible.

Acknowledgments

We would like to thank N.-H. Vu for laser preparation and M. Albrecht (IKZ Berlin) for TEM characterization. In addition, we are grateful for many helpful discussions with C. Hanke and B. Stegmüller. This work has been financially supported by the EU in the IST project “GSQ”.

Dr. Robert Averbeck
Phone +49 89 234 45469
E-mail robert.averbeck@infineon.com

Dr. Lutz Geelhaar
Phone +49 89 234 47507
E-mail lutz.geelhaar@infineon.com

Harald Hedrich
Phone +49 89 234 49362
E-mail harald.hedrich@infineon.com

Dr. Henning Riechert
Phone +49 89 234 45230
E-mail henning.riechert@infineon.com

Laser-Modulator-Integration: Low Cost Optical Transmitter Chips for Data Rates up to 40 Gbit/s

Introduction

The data rates in optical communication systems are still increasing. Directly modulated lasers face severe problems above 10 Gbit/s and therefore other solutions for optical transmitters are required. The most promising approach is the separation of the light generation and the modulation process, which can be performed e.g. by voltage controlled electro-absorption. Monolithic integrated laser-modulator devices (EMLs) are attracting more and more attention due to their great potential in modulation bandwidth, extinction ratio and chirp, outperforming directly modulated lasers. In addition, they offer important benefits in device compactness and packaging costs, which is especially true for the monolithic integration capability with other devices such as semiconductor optical amplifiers (SOAs). In comparison to stand-alone electro-absorption modulators (EAMs), monolithic integrated solutions allow high optical coupling efficiencies between the individual device segments and eliminate polarization control issues.

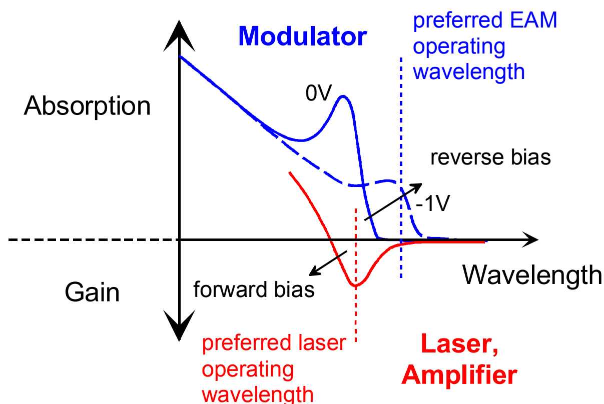


Figure 6: *Qualitative drawing of the optical gain and absorption spectra of a single-type MQW structure driven under forward and reverse bias. For monolithic integration, the offset in operating wavelengths has to be minimized to guarantee optimum overall device performance.*

Because all segments use the same active heterostructure, the major challenge of such monolithic multi-section devices is the proper design of the multiple quantum wells (MQW) for the active and passive waveguides. The goal is to find a design compromise to realize efficient high-speed modulation and low residual absorption of the EAM and low threshold current of the distributed feedback (DFB) laser (Fig. 6).
On the one hand, at the operating wavelength, the MQWs have to provide sufficient optical gain in the forward driven DFB section for lasing operation. On the other hand, the absorption characteristic in the reverse biased modulator section has to provide low residual absorption in the unbiased state as well as high absorption swings under the applied voltage. Therefore, the quantum confined state transition wavelength in the EAM section should be blue shifted with respect to the lasing wavelength of the DFB laser section. In the literature, several approaches such as the epitaxial growth on non planar substrates, removing the active region and re-growing the higher band gap EAM material, disordering the quantum wells, selective area epitaxy or twin waveguide structures have been published. However, all these EML approaches suffer from complex growth and/or fabrication techniques. In order to allow less stringent growth and fabrication requirements, we have patented and are pioneering a single grown double-type MQW approach based on only one common optical waveguide for all device segments as shown in Fig. 7.
Comprehensive modeling of the internal electro-optical effects have shown that this novel kind of MQW layer structure offers the great advantage

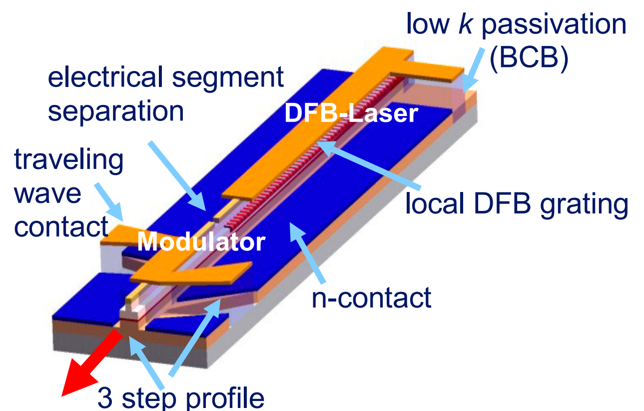


Figure 7: *Device schematic of the fabricated monolithic integrated DFB laser - EAM.*

of simultaneously providing additional optical gain in the laser section and large absorption swings with low residual absorption in the EAM section.
In order to guarantee high-speed EAM performance, the chip layout has been optimized by detailed electrical RF- as well as dynamic electro-optical modeling, resulting in a three step mesa profile and a traveling wave contact design, as indicated in Fig. 7.
In addition, this EML concept has the potential to operate at low EAM driving voltages. This compatibility with SiGe-driver ICs will further scale down the 40 Gbit/s optical transceiver costs.

Layer Structure & Device Layout

The layer structure is grown by MOVPE on a (100) semi-insulating InP substrate. The active area consists of a single grown InGaAlAs double-type MQW stack with three 5 nm thick laser type QWs on the p-side and eight 7.5 nm thick modulator type QWs on the n-side. The QWs are compressively and the barriers are tensile strained. After the first epitaxial growth step a local grating is introduced in the DFB section by holography and wet-chemical etching to define the operating wavelength. In the following second epitaxial step the local grating layer is overgrown by a 1.6 µm thick InP ridge layer and a 200 nm thick ternary InGaAs p-type contact layer. Before starting the device fabrication, a Zn diffusion process is applied for low series resistance. The 2 µm wide ridge waveguide structures are defined by depositing the p-type contact stripes, using lift-off technique, and subsequent standard dry and wet-chemical etching. Self-aligned trenches between the individual device sections allow high electrical isolation with typical values in the order of 25 kΩ. In the following ion beam etching step, using nitrogen, a second mesa is etched to access top side n-contacts and to reduce the pin-junction capacitance along the EAM waveguide. After etching a third mesa step to improve the high-speed performance of the traveling wave contacts, the entire structure is passivated and planarized by benzocyclobutene (BCB). The final front-side process forms the p-type contact pads and the opening of the BCB above the n-type contact pads. Fig. 8 shows a scanning electron microscope (SEM) picture of a fabricated wafer, including EML as well as EML-SOA devices. After wafer thinning and cleaving, the laser and modulator facets are high- and anti-reflection coated, respectively. Finally, the devices are mounted p-side up on Cu heat sinks.

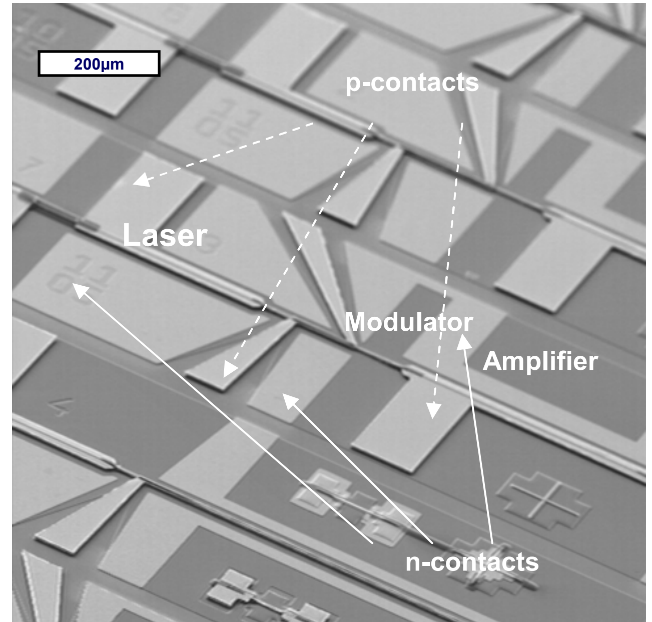


Figure 8: *SEM picture of a fabricated wafer with monolithic integrated DFB laser, EAM and SOA sections.*

Experimental Results

Fig. 9 shows the characteristics of a fabricated InGaAlAs/InP EML in continuous wave operation at room temperature. The optical output power from the EAM facet is measured via a lensed single-mode fiber with a coupling efficiency of about 30 %. The moderate threshold current of 20 mA is correlated with a relative weak grating coupling strength of about 35 cm^{-1}. Operating

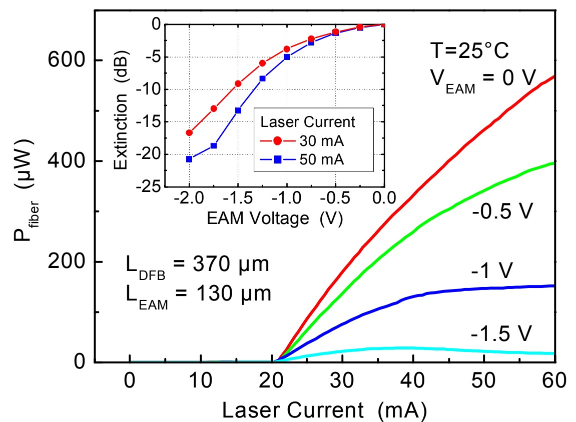


Figure 9*: Measured power-current characteristics of a EML device as a function of the EAM bias, operating at an emission wavelength of 1305 nm. The inset shows the corresponding static extinction ratio for two laser currents.*

the device at a laser current of I_{LD} = 60 mA allows an optical power level up to 570 µW in the fiber. The extracted static extinction ratios (ERs) are reaching values in the range of 17 to 21 dB at -2 V EAM bias and maximum slopes of 13-16 dB/V, suitable for the application of SiGe-drivers.
The dynamic response of the EML is investigated by electro-optical small-signal, Fig. 10, as well as large-signal, Fig. 11, modulation measurements.
In small-signal operation, the devices show 3 dB cutoff frequencies in the range of 29 GHz at 25 °C to 40 GHz at 15 °C. Here, the fiber coupled optical output power is in the order of 0.5 mW, the laser threshold is 31 mA and the

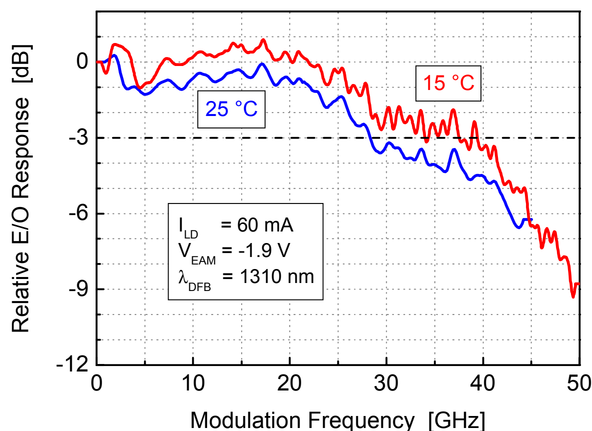


Figure 10: *Measured electro-optical small-signal responses of a fabricated EML device. The DFB laser and EAM sections are 380 µm and 120 µm long, respectively.*

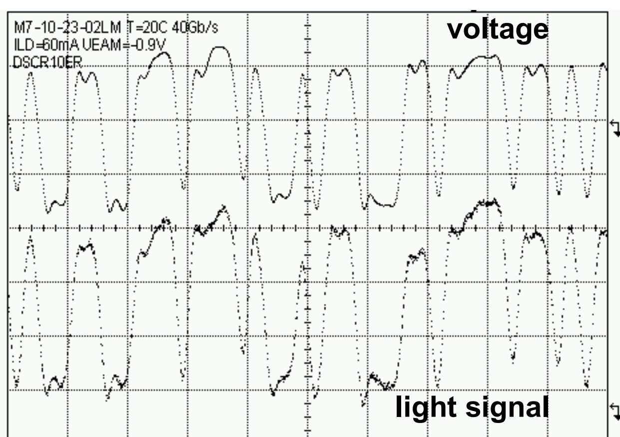


Figure 11: *Measured electro-optical large-signal modulation responses (bottom) of a EML device at 40 Gbit/s. The electrical SiGe-driver signal (top) is shown for reference. The DFB laser and EAM sections are 380 µm and 120 µm long, respectively.*

extracted static extinction ratio is about 9 dB by varying the EAM bias between 0 V and -2 V.
In large signal-operation at 40 Gbit/s, the electro-optical EML response well matches the electrical driver signal, clearly demonstrating its ability to deliver data rates up to the 40 Gbit/s regime. The electrical signal is generated by a SiGe-pseudo-random bit generator provided by CPR HF and is post amplified for the modulator.

Conclusion

Monolithic integrated DFB-laser-modulator devices based on the double-type MQW stack concept are very attractive alternatives to the conventional EML approaches, especially in terms of epitaxial growth and fabrication requirements. The fabricated devices show electro-optical small-signal 3 dB cutoff frequencies in the range of 30 to 40 GHz as well as excellent large-signal modulation responses up to 40 Gbit/s. Thus, the novel double-stack EML approach, fabricated in the InGaAlAs/InP material system, has the potential to meet the requirements of future 40 Gbit/s applications. In addition, the modulator voltage can be provided by high speed SiGe-driver chips, paving the way for high-speed low-cost optoelectronic transceivers.

Outlook

The monolithic integration of an SOA to boost the optical output power, the demonstration of a SiGe-driver EML combination as well as the adoption of the EML concept at 1.55 µm emission wavelength are under way. The results are also under transfer to the Fiber Optics GmbH for commercialization.

Acknowledgments

The authors would like to thank Josef Rieger and Jörg Adler for assistance in technology. This work is supported by the German Federal Ministry of Education and Research (BMBF) under “MultiTeraNet” (01 BP 272).

Dr. Christian Hanke
Phone +49 (0)89 234 49364
E-mail christian.hanke@infineon.com

Dr. Thomas Knödl
Phone +49 (0)89 234 48471
E-mail thomas.knoedl@infineon.com

Dr. Bernhard Stegmüller
Phone +49 (0)89 234 41205
E-mail bernhard.stegmueller@infineon.com

Photonic Crystal Structures

Components for Optical Networks

Photonic crystals are periodic structures with repetition periods in the order of the wavelength of light. 2D hole structures etched into semiconductor heterostructures are compatible with semiconductor technologies. Omitted rows of holes act as optical waveguides and additional holes may be inserted as integrated optical resonators. The project was started to assess the potential of an emerging technology to realize extremely compact components and integrated optical and integrated resonators for optical communications.

During the last years, we have pushed the photonic crystal technology by examining a widely tunable laser and a tunable compensator for chromatic dispersion as relevant active and passive components. The work was done within a BMBF project cluster "HiPhoCs" [91] and in close collaboration with the university of Würzburg (Prof. Forchel).

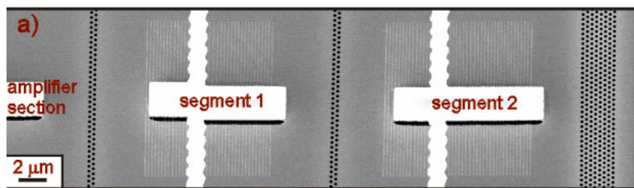


Figure 12: *SEM-photograph of a two segment laser integrated with an optical amplifier.*

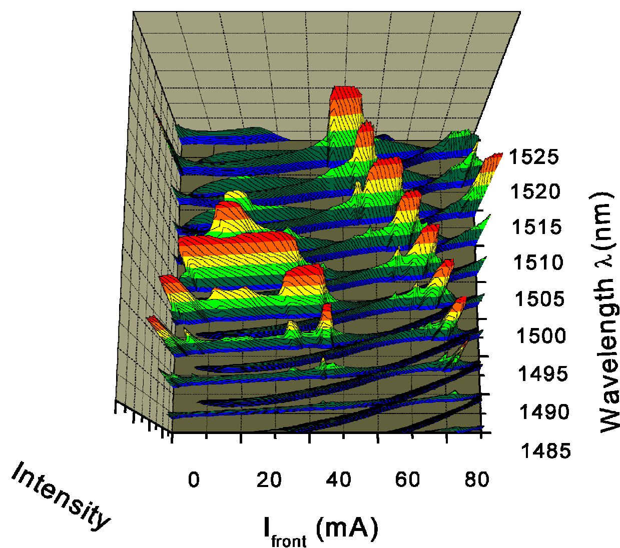


Figure 13: *Measured emission spectrum vs. front segment current for a two-segment laser.*

The two segment lasers (Fig. 12) are using photonic crystals for the front and rear mirrors and the mirror separating the two laser sections. In addition, the laser is covered with binary super-imposed gratings which each define 10 modes spaced 3.1 and 3.3 nm apart, respectively. The devices (Fig. 13 shows a tuning characteristic) are able to address more than 50 wavelength channels within a spectral window of 25...30 nm around 1.52 µm, i.e., a single device is able to fully address the WDM-channels according to the ITU-standard within the amplification band of an erbium doped optical amplifier [92]. The integration of the semiconductor optical amplifier [93] allows to stabilize the optical output power at 5 mW for all wavelength channels.

The improvement in technology leading to a reduction of losses of photonic crystal waveguides to 1.5 dB/mm made it possible to realize thermally tunable dispersion compensators on the basis of photonic crystals based on optical resonators of high finesse [94]. The device with a length of only 420 µm exhibited a chromatic dispersion span of >400 ps/nm which allows to dynamically compensate the dispersion of more than 20 km standard single mode fiber (see Fig. 14). Thus, a record dispersion efficiency of up to 500 ps/nm/mm (for comparison: fiber Bragg gratings offer <1 ps/nm/mm) has already been obtained.

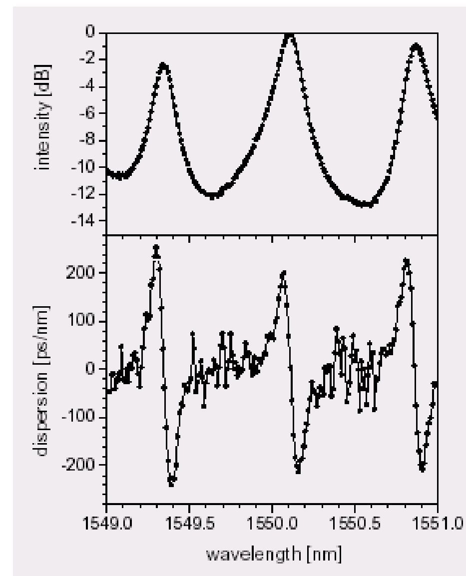


Figure 14: *Relative transmission and chromatic dispersion measuered at a photonic crystal filter.*

Simulation Technology Applied to Phase Masks at MP

Within the BMBF project cluster "HIFoCs" on photonic crystals, the Zuse Institute, Berlin (ZIB) developed novel finite element simulation techniques for the transmission and reflection anlysis of photonic crystal structures with a high refractive index contrast and/or attenuation. A common activity of ZIB, CPR and MP was started to find out, whether the new frequency domain solver offers the same advantage for the simulation of light transmission through alternating and attenuated phase masks.

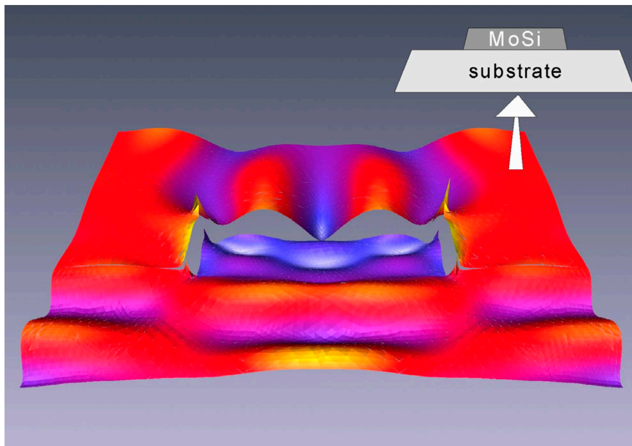


Figure 15: *Electric power of a p-polarized wave traveling through an attenuated phase mask with periodic lines and spaces.*

In contrast to the competing finite difference time domain (FDTD) method, the new type of edge-element solver makes an omnidirectional transient frequency domain analysis **[95, 96]**. As a consequence, it offers the same accuracy at a significantly reduced computational effort.

A set of 2D and 3D benchmark examples defined by MP is currently examined by using a recently implemented C++ finite element prototype.

Fig. 15 shows, normally incident from its substrate side, the electric power of a p-polarized wave traveling through the elementary cell of an attentuated phase mask with periodic lines and spaces (pitch=1). It becomes apparent, that the edge element 2D solver used for this computation is able to resolve the non-continuous behavior of the electric field at the dielectric boundary between the MoSi structure and its environment.

The second example (Fig. 16) shows a vector plot of the real part of the electrical field just behind the mask for a rectangular elementary cell, i.e, the smallest rectangular cell describing the structure, of a hexagonal 3D arrangement of bars. The optical field at the boundary of the bars exhibits a strong vectorial character which makes a vectorial simulation of transmission indispensible.

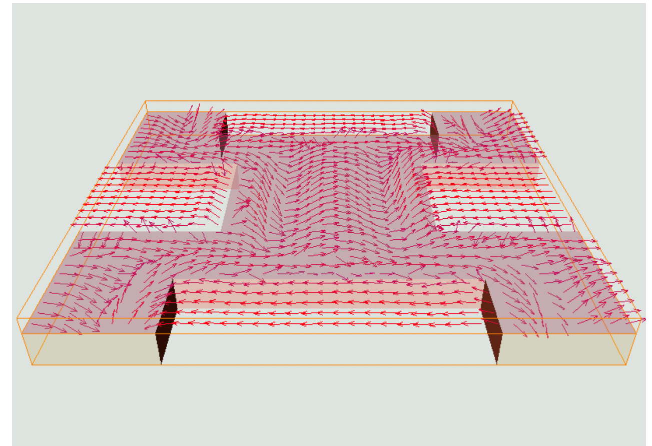


Figure 16: *Vector plot of the real part of the electrical field just behind the mask for a rectangular elementary cell.*

These first computational results indicate that the new algorithms is also superior for mask simulation. The benchmarking with existing tools is currently in progress.

Dr. Reinhard März
Phone +49 (0)89 234-44695
E-mail reinhard.maerz@infineon.com

Systems Technology

The Systems Technology group focus on investigating disruptive SoC architectures, concept engineering for the business units on extending the product road map by means of the latest system architecture platform. Their intention is directed towards using the old platform for as long a time as possible, our goal is to prepare innovative next-generation system architectures and plat-forms, respectively, for the business units COM, SMS, and AI, and prove the feasibility and competitiveness of the new architecture generation.

Depending on the product, the life time of a system architecture is limited up to a few years. As new applications and product features evolve over time, just adding new modules to the old system architecture will seldom do, even if the old system architecture was designed for moduality and openness. Instead, as the new CMOS technology and the new applications call for a new partitioning of HW and SW, the system architecture has to be newly designed. Hence, the new architecture platform will definitely look very different from the old solution: what once was implemented, say, as an accelerator for GSM now becomes embedded software (eSW) to be run on a DSP. Similarly, new video codecs (like h.264) may no longer call for accelerators, but for general-purpose low-power processors, so that former assembler code must be replaced by C code. Or future DSLAM line cards will have to support multiple protocols for the access of wLAN and radio networks, in addition to accessing the home via xDSL techniques, calling for a system architecture with much more flexibility than present in the old architecture.

The main application areas we are pursuing are multi-standard wireless and wired communications, multimedia, robust multi-mode user-interfaces, and driver-assistance systems. After discussions with the BUs about the limits of pre-sent architectures as to evolving applications, the exploration of the design space for a better (costs, performance, etc.) architecture is started. The procedure is as follows: (1) enter the design space at a point that fulfills best the design criteria (area, power, flexibility, simplicity of programming model, scalability, …), (2) explore the design space around this point, i.e. model the architecture quantitatively by profiling the application in iterative fashion, (3) build a bit-true cycle-accurate virtual prototype (preferably SystemC) of the HW-SW architecture for the product class under consideration, and (4) verify function and real-time behavior. In the sequel, we present innovative architectures for multi-standard cell phones (baseband as well as multimedia), DSLAM line cards, and car vision systems.

Generally, performance and power consumption reasons call for next-generation SoC architect-tures with multiple programmable processors which work in parallel on a single application or simultaneously on several applications. Because of flexibility requirements and the ever-growing set of tasks present in the applications, these processors will have to have general-purpose instruction sets, complemented by application-specific instructions. Eventually, these parallel processors will be supported by a few processors with purely application-specific instruction sets. Hence, the evolution will be from heterogeneous towards predominantly homogeneous processor architectures, which is advantageous from the point of view of eSW development. Moreover, terminals like set-top-boxes share major functionalities with next-generation cell phones on the application part. Similarly, the convergence of IT and mobile networks will cause CPEs, STBs and multi-standard cell phones to share functions at layers 1 to 3. Consequently, the convergence of applications on diverse terminals will inevitably lead to a convergence of architectures.

As a result, the former HW-dominated system design is becoming strongly balanced by eSW design. Because of complexity reasons as well as cost concerns, application and architecture (HW&SW) must be modelled separately. Then, the main challenge for eSW for SoCs is the automatic mapping (i.e. code generation) of objects from the application modelling to objects of the system architecture modelling, and progress in system verification. This new design methodology for semiconductor companies and their customers we have just started to explore.

Our work relies heavily on the readiness of people from academia (TU AA, Uni. Paderborn, TU Dresden, TU München, UC Berkeley, ETH Zürich) to research pieces of the applications, SoC architectures and eSW we have selected, and to help us integrate their work into ours. We like to thank them.

Prof. Dr. Ulrich Ramacher
Phone +49 (0)89 234-41296
E-Mail ulrich.ramacher@infineon.com

Multi-Standard Baseband Platform

In contrast to today's dual-band single-standard cell phones, future wireless terminals will have to be multi-band, multi-standard and able to do handover between multiple standards and execute them concurrently. As with the further evolution of 2-4G the plethora of standards will be combined into powerful super-standards like WCDMATDD and HSDPA - these super-standards varying with world regions – the system architect's task is under-going a big change. In the recent past, the design criteria were chosen with regard to what could be realized economically with 0.5 – 0.13µm CMOS technologies. This lead to architectures with minimal area and power consumption. Macros absorbed the compute-intensive signal-processing parts of the physical layer whereas layer-1 control processing was executed on a DSP. With the advent of new standards and the shift to ubiquitous communication, continuation of this style of design would have meant to increase the number of macros to an intolerable height.
Instead, the idea emerged of emulating the macros by a small number of reconfigurable data path units with adjacent small control units.
This way, the firmware increased significantly, the programs could be written by the designers of the chip, only, and the customer had to be involved into the partitioning of the system into hardware and software. Furthermore, the size as well as the number of these data paths would grow with the number of standards and applications, which, in turn, would increase control overhead and area, let alone the complexity of the programming model. This innovative architecture style had been first picked up by startup companies (Quicksilver, Morpho Technologies, Morphics, Mercury, Picochip, to name a few). A success story for reconfigurable computing and communication is still lacking, however. Not only are area and power consumption inferior to alternative architectures – there is no approach at hand for programming reconfigurable architectures in the wake of ever-increasing demands for flexibility.
Thus, to develop an architecture for UMTS at 384 kb/s, CDMA2000 1x DV, GSM/GPRS/EDGE class 12, IEEE 802.11b, IEEE 802.11g (at reduced data rate, e.g. 24 Mb/s), Bluetooth, DAB and GPS, as requested by Siemens ICM TI, it was imperative to pursue new ways.

After agreement has been reached on a reasonable upper limit for area and power, say, 40 mm2 and 200 mW for execution of UMTS or 802.11b, alternatively, we proceeded to design an architecture which is aimed at highest flexibility and simplest programming model.
This way, we arrived at a solution based on a cluster of 4 single-instruction multiple-data (SIMD) DSP cores accompanied by processors accelerating FIR filtering and channel decoding which account for almost half of the total processing power of the entire SDR platform. The processors are connected to shared-memory via a multi-layer system bus. The entire platform is controlled by a general purpose ARM core. For details of the architecture and programming environment, we refer to [97]

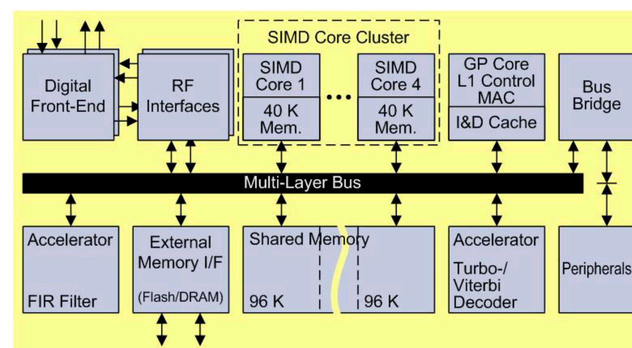


Figure 5: *Multi-standard baseband platform.*

A virtual prototype of the baseband platform is available in SystemC. This way, extensive profiling of 802.11b has been completed and shown the viability of the architectural ansatz. The next step is the design of a real prototype, which will be done in cooperation with SMS and external partners.
As a multi-standard baseband architecture can not be developed without the know-how of the algorithms for the various standards, the interface between customer and SMS will need to be redefined: a common modeling of the applications (the various standards), which is independent of the architectural realization, will become the basis for the system specification. To this end, CPR ST has formed a working group with members from AMD, Alcatel, Lucent, Nokia, Siemens COM and Philips.

Dr. Hans-Martin Blüthgen
Phone +49 (0)89 234-53178
E-Mail hans-martin.bluethgen@infineon.com

Digital Circuits: Key components for Cognitive Radio

Motivation and Definition of Cognitive Radio

During the next years, explosively growing demand for wireless communication capabilities will result in a shortage of available spectrum in so called "hotspots". However, measurements showed that a lot of spectrum, licensed and unlicensed, is unused depending on place and time. Cognitive Radios (CR) are an approach to resolve this dilemma. A Cognitive Radio is a radio frequency transceiver that is designed to intelligently detect whether a particular segment of the radio spectrum is currently in use, and to jump into (and out of, as necessary) the temporarily-unused spectrum very rapidly, without interfering with the transmissions of other authorized users (IEEE definition). A Cognitive Radio therefore has to be aware of the activity and the availability of spectral resources within its operation range and it has to be able to characterize the spectral activity it is sensing. The latter requires multi-band and multi-standard capabilities – similar to next-generation cell phones (4G).

Joint Cognitive Radio Project

Infineon is going to participate in a joint Cognitive Radio Project between the Berkeley Wireless Research Center and several industry partners. The research fields addressed in this project include the physical layer functions (sensing, channel estimation, data transmission) and the link layer (group/link management, MAC) of a Cognitive Radio system.
Besides Infineon's activities on the digital baseband processing including the application modeling and the HW/SW architecture development, we will focus on the concept and design of key building blocks like the analog-to-digital converter (ADC). ADCs are crucial for the feasibility of a Cognitive Radios and they have a huge influence on the overall system performance. The tough design requirements for performance, resolution, and power dissipation can hardly be met with existing technologies. In addition, the cost pressure requires the converter to be manufactured in a standard deep-submicron CMOS technology and to be integrated on the same die as the digital baseband processor thus causing problems with parameter variations and noise induced by the digital environment. The basic idea to overcome these issues is to spend effort in the digital correction of imperfect analog circuits. In a recent project, CPR FEC and CPR ST made use of this approach, resulting in a 4 GS/s, 6-bit flash converter for hard disk drives [98]. At the Berkeley Wireless Research Center, a 0.5 GS/s, 12-bit ADC has been developed recently that equalizes the erroneous results of a fast converter by using an adaptive digital filter controlled by a much slower reference ADC [99].

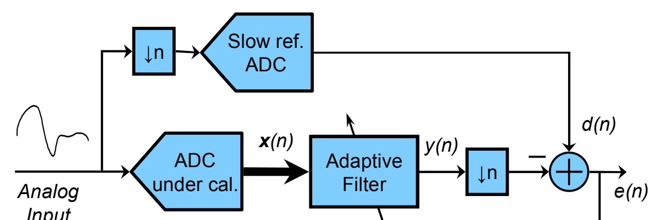


Figure 7: ADC with background calibration in the digital domain by adaptive filtering.

Nikolaus Brüls
Phone +49 (0)89 234-40322
E-Mail nikolaus.bruels@infineon.com

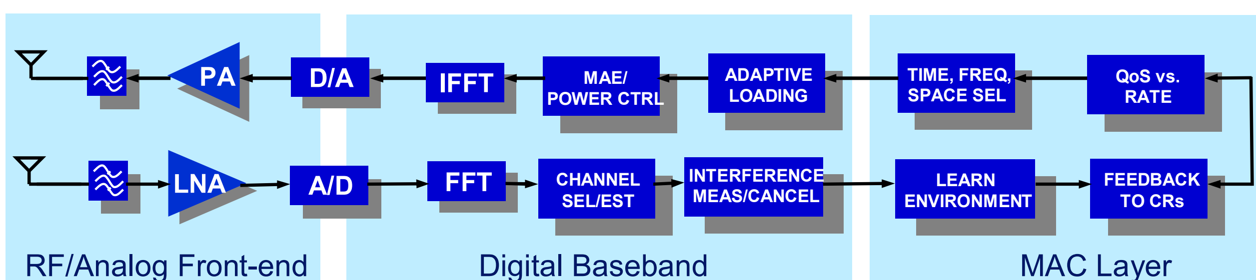


***Figure 6** Functional block diagram of a Cognitive Radio.*

Embedded Multimedia Processor for Smart Phones

Emerging high speed wireless transmission standards (2.5G, 3G, WLAN) will extend the range of applications of today's voice dominated mobile handsets. The usage as data terminals will have a huge impact on future processor architectures for these devices. We're just starting to see Smart Phones containing a PDA which provides internet access, hand writing and speech recognition, still and moving picture camera functionality, voice and video telephony services, music play back, games and many other applications. As in desktop computers, standard operating systems as WindowsCE or Symbian convert mobile terminals into universal platforms which run programs from arbitrary software manufacturers.

The increase of desktop computer performance is mainly reached by the increase of clock frequency and cache sizes. In only a few domains specialized hardware accelerators are established (MMX, graphics accelerators). This solution is flexible at a maximum and keeps costs for software development low. On the one hand, power dissipation and costs of these systems are much too high for usage in mobile devices, on the other hand, programmability and flexibility need to be maintained for many multimedia applications which are emerging in mobile devices. Additionally, in future, independent software manufacturers will provide customized, value adding applications for the camera equipped mobile terminals. Already now, this is the case for PDAs. Since these software manufacturers won't adapt their programs to different processor platforms, on the long run, an application processor has to support a standardized instruction set.

The stringent requirement for low power consumption demands for low clock frequencies, which, in turn, is only possible with parallel processor architectures. Various architectures were explored by CPR ST, covering Very Large Instruction Word (VLIW), Single Instruction Multiple Data (SIMD) and Multiple Instruction Multiple Data (MIMD) processors. Pure SIMD architectures provide very good performance /power ratios, but their flexibility and programming models are too weak for this domain. MIMD architectures provide a sufficient performance/power ratio and are best suited for instruction set compatibility, but adapting applications to multi processor architectures is a hard task and can't be automatically performed by a compiler. VLIW architectures which are extended by SIMD media instructions also provide a good performance/power ratio and have a fully compiler based programming model. However, the instruction set of a VLIW processor can not be natively compatible to the ARM instruction set, which is the de facto standard for mobile phones and PDAs. In order to overcome this blocking point for innovation and differentiation, the binary compilation technology will gain in importance. This technology enables the automatic translation of an application which is available in a standardized executable format – e.g. ARM or Java byte code – into a new executable format for an innovative processor.

CPR ST developed and evaluated a general purpose VLIW architecture [100]. The semantics of its extendable instruction set is similar to the semantics of ARMs instructions in order to simplify the binary compilation process. Media instruction set extensions provide for additional performance in regular data processing loops, which are inherent in many video, audio and image processing algorithms.

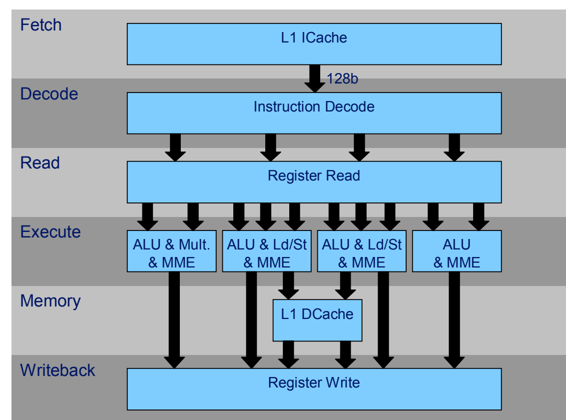


Figure 8: *CPR ST's VLIW Core with 4 general-purpose execution units.*

The discussion with SMS is still on-going. Also, we are taking part in the assessment of multimedia co-processors by SMS CE. A decision and selection, resp., is expected to be taken in the course of the business year 04/05.

Ulrich Hachmann
Phone +49 (0)89 234-42974
E-Mail Ulrich.hachmann@infineon.com

Access Processor Platform

A major focus of Infineon's wireline communication (COM) products is the network access segment. In this segment flexible, yet cost-effective solutions are required to deal with emerging trends, such as Internet Protocol (IP) for the first mile and Quality-of-Service.

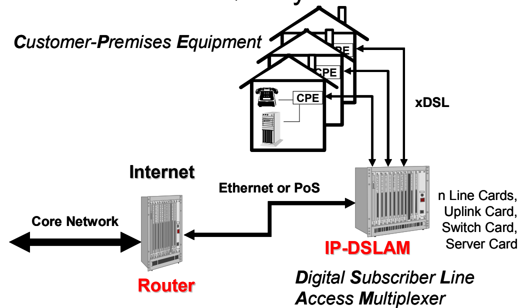


***Figure 9:** IP-DSLAM and CPE deployment scenarios for wireline communication products.*

In a series of workshops a team of experts from system engineering, technical marketing, business development, research, and development identified the need for a next-generation product platform that is tailored to the growing requirements of the access domain and can easily be programmed by the customer. Consequently, a joint project has been set up to develop a suitable system architecture.

There are three challenges in designing next-generation access processors that the project focuses on: 1) developing benchmarks, workloads, and reference implementations for packet-processing algorithms and protocols, 2) profiling the applications and iteratively refining architectural building blocks to such a degree that the relevant parameters of the design space can be determined, and 3) defining the architecture development platform including a natural programming model.

Clearly, to develop appropriate programmable architectures, a careful application analysis and a well defined benchmark are required. The availability of system-level benchmarks, however, is still an unresolved issue. Especially in the access domain, no established benchmarks exist. We have therefore developed a complete system-level benchmark including functional, traffic model, and environment specifications. This benchmark represents a future IP-based DSL access multiplexer (DSLAM) anticipating higher layer protocol processing, traffic management, and increased throughput [101]. We describe our IP-DSLAM benchmark in a modular and architecture independent way using MIT's Click, a framework and language for composing packet processing applications. Preserving the front-end we ported it to embedded processors and currently assess its use as programming model [102].

As a starting point for the profiling and architecture refinement step, we use a number of embedded general-purpose processors, such as MIPS, ARM and PowerPC, as well as packet processing engines like the PP32 and our N-Core. The packet processing engines provide high performance, whereas the general purpose processors have mature compilers.

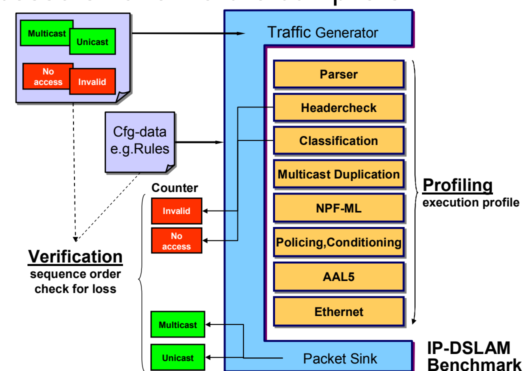


***Figure 10:** IP-DSLAM system-level benchmark.*

Using the benchmark we profiled the combination of core and compiler in order to identify optimization potential. This either leads to specialized instructions (that can still be used by the compiler) or loosely/tightly coupled co-processors.

These optimizations need to be traded off at the multi-processor level with the number of required processor cores. Thus, the 2nd phase of design-space exploration considers the reference implementation mapped onto a multiprocessor system containing cores, accelerators, memories, interconnects, and interfaces [103]. So far, we identified a number of useful ISA extensions and co-processors. Currently, we are in the process of evaluating mul*tiprocessor topologies for the definition of an initial platform architecture.

In the next step, the platform architecture will be assessed for its feasibility in Customer Premise Equipment (CPE). Besides COM AC and CL AA, several universities are contributing to the project: HNI at Uni Paderborn, TU Munich, and UC Berkeley.

Christian Sauer
Phone +49 (0)89 234-53979
E-Mail christian.sauer@infineon.com

Robust System Architectures for Embedded User-Interfaces

Motivation

Investigating the current market for information-, communication- and consumer electronics, an interesting observation can be made: the devices are equipped with more and more functions and features and, simultaneously, the diversity of user groups increases. The ever growing feature list contains voice-, text- and video-communication, web-surfing, personal information management, recording and playback of music, photos, video and radio. The average user, however, is totally over-whelmed with the operation of these functions. In the mobile communication industry, this effect is known as the *Usability Gap* [104]. The usability gap is expected to have a growing negative influence on the sales figures: already now the average customer uses less than fifty percent of the features of his/her cell phone. Accordingly, the manufacturers will have growing problems to convince the user of the necessity of new functions if they are too complicate to operate. This problem is not unique to mobile communication: the manufacturers of feature-loaded DVD-recorders, digital photo-cameras, washing machines and modern cars stuffed with electronics suffer from the same effect.
An obvious way out of this dilemma is the improvement of the user interface and the integration of assistive functions which are easy to operate and adapting autonomously to the user's preferences and level of expertise. The underlying complexity of the functions should be hidden from the user and the devices should be operated through a standardized assistive interface using robust natural communication channels.
As the man-machine-interface problem is essential for the future business of SMS and AI (cell phones, driver-assistance systems), we have formed three projects: (1) Dialog-Modem, (2) Car Vision System, (3) Robust Pre-Processing of sensor information for speech and vision.
The final goal of the projects is the development of a robust SoC architecture platform. As the first step, we need to model and profile the applications, then derive the requirements as to performances, power, programmability and alike. It is this first step, we are reporting here.

Dialog-Modem

The aim of this project is the improvement of the ease of use and the robustness of man-machine interfaces for cell phones, PDAs and alike, by integrating multiple different communication channels. Like in the human-to-human dialog, fusing audio- and vision channels enhances the robustness of the information transfer between man and machine.
As a first demonstrator, we have integrated several communication channels for an inter-active e-commerce scenario:
- An audio-visual recognizer based on the combination of an off-the-shelf HMM-speech recognizer with a lip-reading algorithm. We could show that in noisy environment the speech recognition rate is greatly improved compared to an audio-only recognizer [105].
- A robust face tracker based on the fusion of the skin's colour and the face's shape. We use this tracker for gaze following and for the "virtual camera-man": an algorithm which zooms on the face of a person in a free-hands video-telephony application.

Figure 11: *Virtual Camera-man.*

- A pointing-gesture recogniser which is based on the fusion of skin colour and hand movement. We can select and move objects on a computer screen just by pointing at them [106].
- An animated anthropomorphic 3D head model with lip-synchronous speech output and mimics control. This model represents a "Virtual Personal Assistant" (VPA) which acts as a sales assistant in the e-commerce scenario [107].
Based on a complexity analysis of these channels, we have calculated a sum of about 10.000 MIPS for the fully fledged VPA. For embedded applications, this requires a processor platform which exploits the inherent task- and data-parallelism of the different communication channels.
Next steps on our application roadmap are (1) the development of a client-server model and the implementation of parts of the VPA in a mobile device ("Mobile Virtual Assistant"), and (2) its integration into a driver assistance system.

Car Vision

A major challenge for automobile designers is to improve driver safety and comfort. Here, the interpretation and understanding of video sequences is one of the key technologies for driver assistance systems. First camera based applications like "lane departure warning" or "blind spot checker" are already introduced in the automotive market. Today's car vision systems are limited to a single functionality, which requires only small fields of view or the processing of a few image regions. The next generation has to support all possible applications depending on the camera direction, which requires the understanding of more complex traffic scenarios (urban traffic, intersections, …) and the improvement of robustness (all day, all weather) as well as the reliability. Therefore a strong increase of the required computational performance is expected. To avoid an expensive infrastructure for data communication, it is reasonable to locate the image sensor and the processor as close as possible. This justifies the development of vision processors, which offer high computational performance at reasonable costs and will fit to the limited mounting space and extreme environment temperatures.

Vision Processor

Typical for vision applications is the high amount of data parallel processing on low-level and the parallelism of tasks in the medium- and high-level. Therefore, parallel architectures are well suited to offer the necessary computation at low clock frequencies. CPR ST presented a first vision processor in 2001: a SIMD-architecture with 16 processing elements (106 GOPS@200 MHz) [108]. Currently, the SIMD-architecture is going to be expanded to a scalable multi-processor architecture, which consists of SIMD-cores as well as of general purpose processor cores. The scalable multi-processor approach offers optimized processors for different application requirements and supports SIMD, MIMD as well as sequential processing. A virtual prototype of the multi-processor architecture as well as an optimizing SIMD compiler is available.

Application Software

The programming interface should support a comfortable application development as well as the reuse of existing application software (mostly written in "C"). A library of image processing functions is provided to allow a comfortable use of functions with an optimized performance and a reduced data I/O. ST develops new efficient approaches for motion estimation, object detection and tracking, which can be used in applications like the "overtake-checker" or a "door-opener-assistant" [109]. The integration of application specific tasks into the image processing library will increase the attractiveness of the vision processor as well as the added-value for IFX.

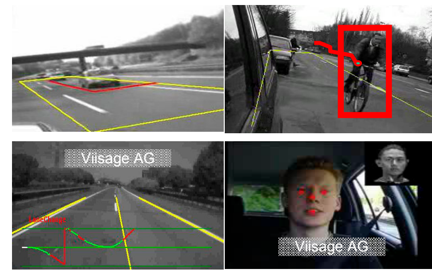


Figure 12: *Car vision application scenarios: overtake checker (a), door-opener-assistant (b), lane-change-assistant (c), cockpit-monitoring (d).*

Robust Pre-Processing

Whereas the focus of the two preceding projects is on the *integration* of existing solutions in audio- and vision processing, this project presents new methods of extracting more information from the sensory data than can be obtained with classical methods.

Speech processing

Mobile communication devices challenge automatic speech recognition systems (ASR), as they are often used in environments with loud background noise. On the other hand, recognition accuracy of today's ASR drops dramatically if speech signals are corrupted only with small amounts of noise. At CPR-ST we therefore investigate the relatively excellent performance of the human auditory system and transfer the principles providing noise robustness to technical ASR. As a test system we applied the AURORA framework, which consists of connected digits recorded from multiple speakers. Several noise scenarios were added at signal-to-noise ratios ranging from 20 dB to -5 dB. One principle we found to enhance recognition accuracy in noise is adaptation in the auditory nerve. Adaptation is a basic principle of neuronal processing which suppresses quasi-stationary signals (like continuous background noise) and accentuates signal onsets, which are typical for speech. Applying our adaptation model to mel-frequency cepstral coefficient (MFCC) feature extraction enhanced recognition accuracy in noise (AURORA 2 task, averaged recognition scores)

from 56.4% to 75.6% (clean training condition). This corresponds to a relative improvement of the word error rate by 41%. Adaptation outperformed RASTA processing, which is applied in almost all mobile communication devices by more than 10%, which corresponds to a relative improvement of 31% [110]. In the next steps, more temporal features will be investigated and corresponding neural architectures evaluated.

Image processing

Applications which are based on image processing demand flexible and modular architectures that process information in a robust way. Inspired from biological systems we developed an innovative signal processing architecture based on pulsed signal generators (neurons) coupled by dynamic weights, which adapt their coupling strength dependent on the information presented to the system. Dedicated functions for robust information processing can be realized in a flexible way by defining connections between individual signal generators as well as by assigning adaptivity to the coupling weights. Architectures for image segmentation, low-level feature extraction based on Gabor-Wavelets measured in the human brain [111], and object detection were successfully implemented [112].

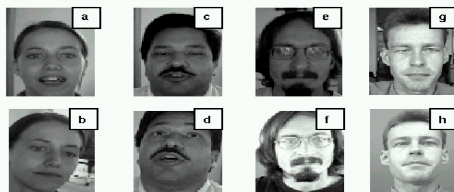


Figure 13: *Application scenario face-detection. The face-detector has to detect faces under a variety of conditions: change in pose (a,b,c,d); change in illumination (e,f); different backgrounds (g,h).*

To prove robustness application scenarios for face detection as well as for head tracking were defined. For face-detection a general face mask was derived which is based on four different Gabor wavelets as well as non-linear post-processing by detection of local maxima of amplitudes in the feature domain. The performance of the face-detector was measured with respect to resistance against pose variations (Fig. 9 a,b,c,d), changes in illumination (Fig. 9 e,f) and the presence of different backgrounds (Fig. 9 g,h). Compared to state-of-the-art solutions, based on the detection of Gabor-wavelet amplitudes only, the non-linear post-processing enhances the sharpness of the detector's response characteristics significantly (Fig. 10). Here, the variation of the response characteristics was reduced by 60% resulting in a significantly improved robustness for face-detection.

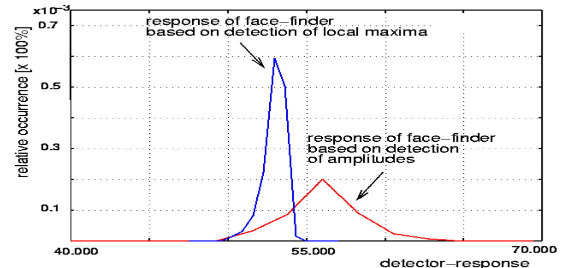


Figure 14: *Measured statistics of the face-detector's response. 1500 different faces were applied to the detector; red curve: state-of-the-art detector using gabor-wavelet amplitudes only; blue curve: face-detection based on detection of local maxima.*

To provide real time capabilities and low power consumption for embedded application like robust head tracking in cell phones, analogue circuits (130nm C11-technology) as well as a 3D-stacking technology were developed in order to integrate massively connected neural layers of the architecture. Test chips with 16k neurons and 65k synapses and 20mW power consumption were realized [113].

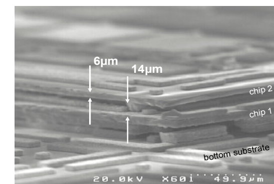


Figure 15: *3-layer test-device.*

3D-stacking of thinned dies with a residual thickness less than 10µm is the key to realize large networks of coupled pulsed neurons. The 3D-stacking technology offers more than 360 vertical contacts per mm², each contact has an area of less than 5x5µm^2 [114]. The 3D-stacking technology is an extension of SMS's F2F-technology to three dimensions and was developed at CPR ST in cooperation with SMS and the University of Ulm.

Dr. Axel Steinhage
Phone +49 89 234 55181
E-Mail axel.steinhage@infineon.com
Dr. Axel Techmer
Phone +49 89 234 40055
E-Mail axel.techmer@infineon.com
Dr. Werner Hemmert
Phone +49 89 234 53055
E-Mail werner.hemmert@infineon.com
Dr. Arne Heittmann
Phone +49 89 234 52067
E-Mail arne.heittmann@infineon.com

SoC Design Framework

Next-generation SoC architectures for products, such as cell phones and CPEs, will comprise multiple processors which work in parallel on a single application or simultaneously on several applications. In order to guarantee re-use over various architecture platforms and well-timed development of HW and eSW the complexities of these architectures call for separate modeling of application and architecture. Whereas tools and methods for modeling a HW architecture have made impressive progress, those for eSW lag behind. The main challenges for eSW for SoCs is the automatic mapping (i.e. code generation) from the programs of the application modeling platform to the HW/SW objects of the architecture modeling platform, and progress in system verification.
The SoC design framework project aims at the assessment and combination of available design tools and their extension for missing functionalities [115]. The requirements for the assessment are derived from the modelling problems which we encounter in our advanced SoC projects (Fig. 11). Tool environments like Metropolis, Ptolemy and Simulink are assessed for their applicability in the system design process and are extended where they do not cover the desired design flow sufficiently.

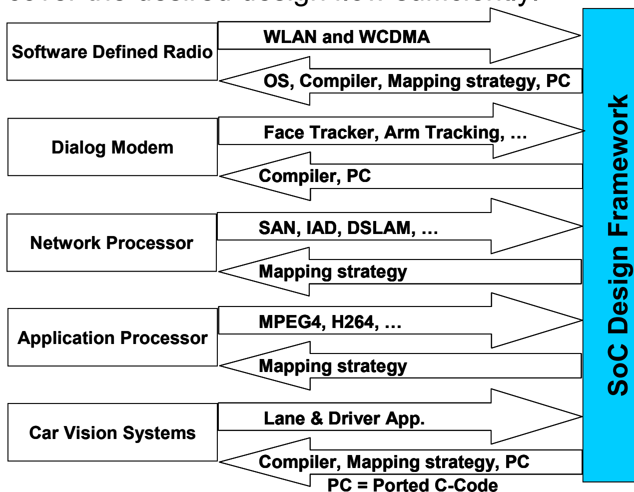


Figure 16: *SoC design framework is driven and supports concrete system developments.*

An example for such an extension is the semi-automatic generation of multithreaded source code from an application model produced from, say, Simulink. This way, an abstract system model is obtained. Upfront to the code generation runs a partitioning of the system for a mapping onto a given multiprocessor architect-ture (see multi-standard base-band project, for example).

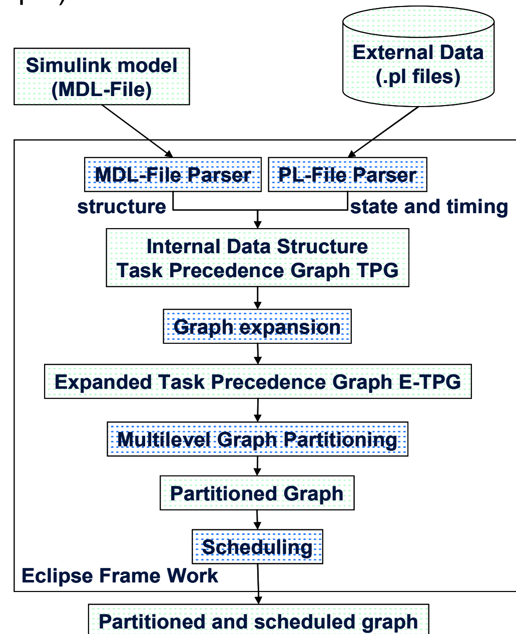


Figure 17: *Partitioner and static scheduler.*

Partitioning onto parallel processors

To handle task-level parallelism, the system model needs to be partitioned and scheduled onto parallel target architectures. Approaches based on graph partitioning and optimization techniques like integer linear programming and branch and bound algorithms are used. The graph is extracted from a Simulink model and enriched by information, like the runtime of each function.

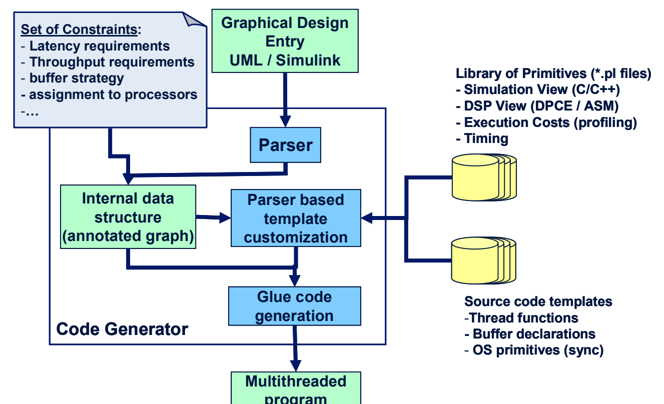


Figure 18: *Code generation from a system model.*

Code generation

The complete system design flow spans multiple abstraction levels. Hence the system description has to be transformed multiple times – always towards the target architecture.
For the top most transformations often the term "code generation" is used, as a lot of code which will be compiled by compilers of the target hardware architecture is generated from the abstract application model.

Compilation techniques

As soon as the code for the target architecture is generated in a high level programming language like C, C++, C#, Java or high level programming languages with parallel extensions like Data Parallel C Extensions (DPCE), the compilation to the target needs to be done. For non-standard architectures or parallel processors, it is very challenging to provide efficient compilers, which help to avoid manual coding of assembly. To allow modifications to the hardware architecture, a generation of the compiler based on an architecture description is desired. Therefore compiler generation tools like CoWare-Lisatek are assessed. Additionally, compiler development for parallel architectures is addressed by own development efforts. As part of the project a SIMD-compiler was developed, which allows to change architectural parameters within a wide range (e.g. the number of processing elements of the SIMD processor). It is used for multimedia applications and car vision systems.

Tool assessment and extension

Metropolis, developed at UC Berkeley, is one of the rare design frameworks which addresses both application and architecture modeling, and even with the same meta-model. It supports simulation, formal analysis and synthesis.

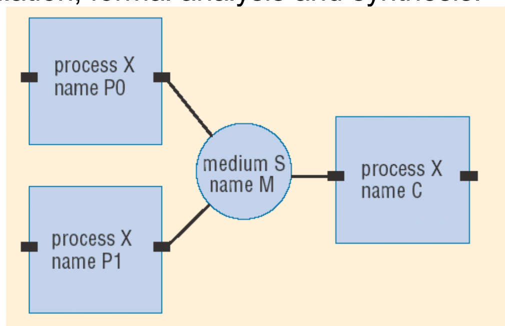


Figure 19: *Metropolis Functional Domain.*

Applications are described in the functional domain by means of concurrent processes which communicate via media, as shown in the example (Fig. 4). The strict separation between computation, realized in the processes, and communication, realized in the media, facilitates reuse of process objects.
A specific architecture on the other hand is described by its services, which are offered to the functional domain. Services are described again by processes, communicating via media, just as on the functional modeling level, an example is shown below. The resulting networks in the architecture domain usually correspond to the real physical structures of implementation platforms. The association between the functional and the architecture modeling level is reached by means of a mapping network. The strict separation of the mapping from the modeling domains facilitates experiments for hardware and software design space exploration [116].

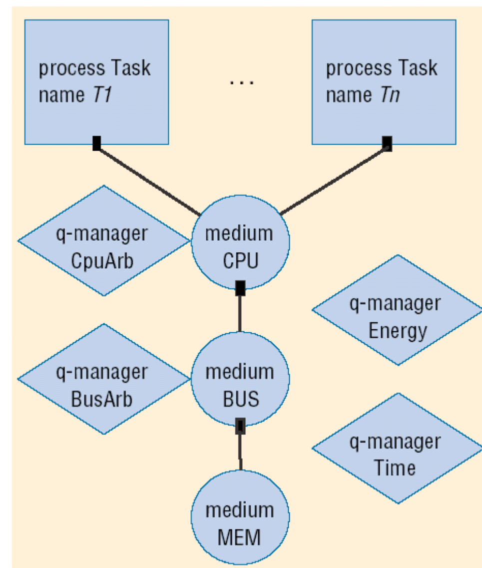


Figure 20: *Metropolis Architecture Domain.*

As combined application and architecture modeling is an open research issue, CPR ST has started a cooperation with the Center of Hybrid Embedded Software and Systems (CHESS) and the Berkeley Wireless Research Center (BWRC) from the University of California, Berkeley. The goal is to create a common framework for application and architecture modeling for two sufficiently different product classes: multi-standard cell phones and customer premises equipment.

Dr. Cyprian Grassmann
Phone +49 89 234 53074
E-Mail cyprian.grassmann@infineon.com
Jens Harnisch
Phone +49 89 234 54667
E-Mail jens.harnisch@infineon.com

Emerging Technologies

Ambient Intelligence - Industrial Research on a Trendy Concept

Ambient Intelligence is the vision that technology will become invisible, embedded in our natural surroundings, present whenever we need it, enabled by simple and effortless interactions, attuned to all our senses, adaptive to users and context and autonomously acting. High quality information and content must be available to any user, anywhere, at any time, and on any device.
Some believe 'Ambient Intelligence' is a vision for the far future: we may be surrounded by various fantastic features such as intelligent electronic wall papers or 'smart dust' forming distributed intelligence with spectacular features. Indeed, *such* visions lie at least 20 years ahead of us. They will require major progress of alternative technologies that have presently not even shown basic feasibility, such as large-size paper-like display technologies. Experience tells that the introduction to the market of new basic hardware technologies takes a long time even after functionality-proof is accomplished.
On the other side, already today indications of a trend towards ambient intelligence are evident. While in the 1970s one computer served many users, and in the 1990s the personal computer served humans on a one-to-one basis, today more than one computing device serves each user. Peripheral devices which were rather dependent on central computing power a few years ago now contain powerful own computing devices. This trend towards distributed electronic intelligence will likely prevail in the near future. Many interesting aspects of 'Ambient Intelligence' are relevant in this context. They are feasible by today's technologies or need only limited innovation in sub-fields such as packaging or chip placement. They are based on existing hardware technology and may be products in 5-10 years.
In addition, other preconditions for the relevance of industrial research must be kept in mind. We head for applications that make sense to the customer and fulfill real needs. We strive for markets with a sufficient size in order to pay for the R&D effort. The projects in the 'Emerging Technologies' department of 'Corporate Research' head for various aspects of application-oriented research in the context of 'Ambient Intelligence' or 'Ubiquitous Computing' as it often called.

One project heads for electronics integrated into clothing. This represents nothing but another step towards portability which is envisioned after the successful introduction of notepads and mobile phones. We followed the idea of seamless integration of electronics into clothing. A first demonstrator was presented and resulted in a huge public attention.
A second project was derived from the first integrating electronics into 2D-structures such as carpets or wall papers. A distributed meshed computing network of processing elements is built that uses self-organization and error correction. In this way an intelligent environment is built around individuals responsible for safety, protection and health care purposes.
A third project elaborates on a low-cost wireless network for ubiquitous computing environments that creates the necessary link between the user and distributed electronics. Smart offices and hotel room infrastructures may be among the first examples where this vision will become reality.
Finally, we investigate chances for applications of smart RF ID tags that represent possible solutions for peripheral intelligence. The prime challenge for those devices is the demand for an extremely low cost level which will demand innovation not only on the chip level but along the complete value chain.
The research at the department of Emerging Technologies strives for application demonstrators and technologies that enable semiconductor solutions for the technology lifestyle of the individual in the 21st century. Here, the individual is the subject whereas electronics is object. The users of the targeted applications want to be served by an environment with an excellent interface between technology and the human. The applications are controllable without specific knowledge. It is our vision to provide human individuals with means to enhance and facilitate control of their lives, being assisted by highly-functional electronic appliances in the background.

Dr. Werner Weber
Phone +49 (0)89 234-48470
E-Mail werner.weber@infineon.com

A Wired Peer-to-Peer Network for Smart Textiles Applications

Many promising technologies are emerging in the area of intelligent textiles like electrically conductive yarns or pressure sensitive fabrics [123]. State of the art feature sizes of integrated circuits allow for powerful and yet small and cost-efficient microelectronic devices. Many interesting applications in the field of technical textiles arise by merging micro-systems and textile fabric structures: pressure sensors in floor coverings for alarm plants or motion detection (person tracking), indicator lamps in floor or wall coverings for guidance systems in public buildings, distributed sensor networks for detection of defects in textile concrete constructions, and many more.

Fig. 1 shows a schematic of the Smart Carpet application. Identical modules are connected to each of their four neighbors by interwoven conductive filaments used as data lines or power supply. Several defects may occur within such a wired peer-to-peer network during fabrication or operation: cuts may lead to open lines, modules may be destroyed or missing and most important, a short circuit of several lines may occur. For a high yield in a reel-to-reel production and robust functionality we require fault-tolerance to all those defects.

In addition, the demand for low-cost installation requires that the smart textile can be cut into irregular shape to fit into any given room. To meet those demands we developed the self-organization technique ADNOS (algorithmic device network organization system) [117].

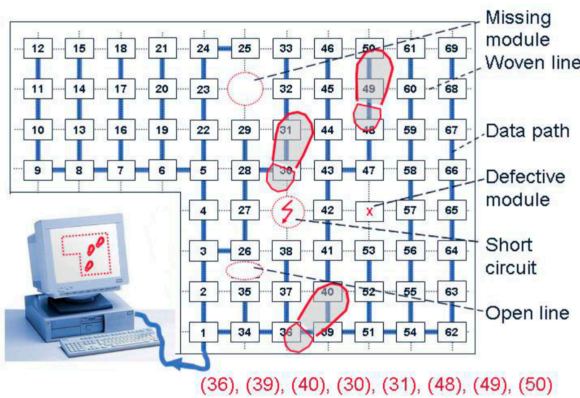


Figure 1: *Schematic of the wired network within the Smart Carpet, showing the automatically numbered modules and routed data paths; the indicated possible defects can be handled by ADNOS; sensor data are sent to the PC.*

The smart textile (Fig. 2) is based on a polyester fabric with interwoven silver-coated copper wires with a line resistance of 0.4Ω/m [126]. To achieve a larger sensitive area for the touch sensor, we embroider a meander-shaped wire. The modules are connected to the crossover points of the conductive lines in a single step using anisotropic-conductive adhesive. The pitch of the woven pattern is 20cm in weft and warp directions, respectively. To reduce mechanical stress of the devices on the PCB, the modules are encapsulated before mounting. The achieved contact resistance is below 50mΩ/contact. Power switches are implemented, each of which is able to switch the current for the complete network. Their resistance is below 150mΩ.

Each module within the network exchanges control messages or sensor data with its four nearest neighbors, and controls and drives a specific region. No prior knowledge about their position within the grid is used. Control data are fed into the network through a portal, which is an arbitrary module that directly connects to the PC.

Before operation, a set-up phase is initiated: Power switches are activated to route power to the entire network. Then short circuits within the network are detected and defective branches eliminated. Next, each module computes its position in the network using information received from neighbors and determines its

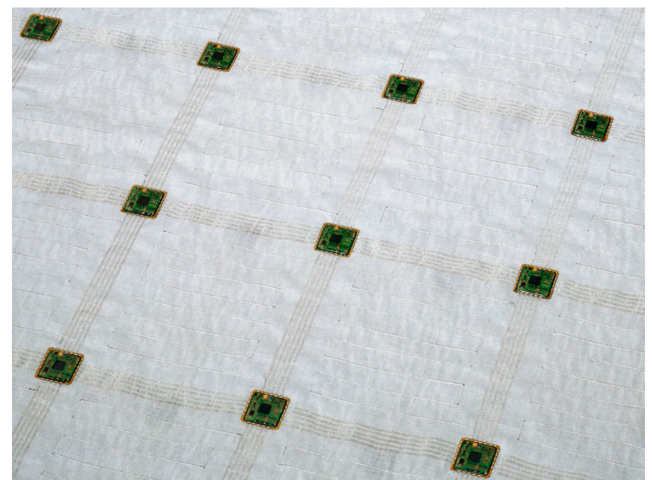


Figure 2: *Microprocessor modules integrated into a fabric with interwoven silver-plated copper wires. The embroidered meander-shaped wires form the sensitive area for the capacitive sensor.*

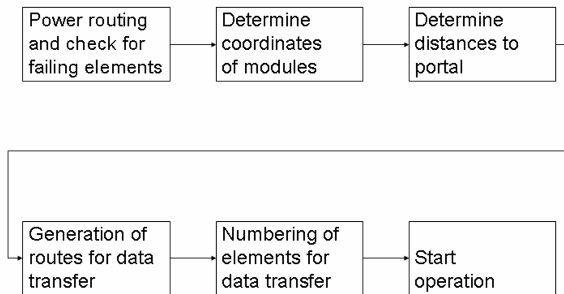


Figure 3: *Power-up and self-organization phases of the ADNOS system.*

distance from the portal. Afterwards, data routes are determined (Fig. 3). The portal then numbers the modules based on the established data routes. This assigns each module to a unique address number. Except for the numbers of its direct neighbors, no additional routing tables are needed inside the network. If new defects are detected, the self-organizing routine is repeated and new routing paths are established. This procedure results in great flexibility in the 2D shapes which are allowed as they typically occur in room floors.

The sensor data from the network are transmitted to the Smart Carpet monitor application. We use an RS232 interface at a data rate of 115200 bps, which could be changed easily into another interface (e.g. USB, wireless). Customized features are defined in the monitor application, e.g. processing and evaluation of sensed data or control of light-emitting diodes.

The Smart Carpet monitor evaluates the incoming data from the network and is fully customized. In case of alarm systems, for example, the user can define a time frame and assign floor areas where sensor signals should trigger the alarm. Additionally, intelligent data mining in the application makes it possible to detect whether a person has fallen down on the floor and lies motionless (Fig. 4). This application is useful for elderly people living alone, as emergency calls to ambulances or medical care providers can be triggered automatically. The application of emergency way guidance (Fig. 5) will be possible, using integrated LEDs.

Enhancing the application software, several independent networks can be combined into an integrated system as they occur in buildings with several floors. Furthermore, the vision of smart rooms with networks of sensors and actuators beneath the wallpaper, under the flooring and on the ceiling comes closer to reality. In future smart rooms, it will not be necessary to install light switches, measuring points for air-conditioning, automatic control for sunblinds, or alarm systems. Smart textiles controlled by powerful software will be a basic technology of ambient intelligence.

The first demonstrator of the smart carpet, featuring 180 modules with capacitive sensors has been presented by Infineon and Vorwerk-Teppiche at the Orgatech 19.10.-23.10.2004 in Cologne.

Christl Lauterbach
Phone +49 (0)89 234-53467
E-Mail christl.lauterbach@infineon.com

Figure 4: *An alarm will be triggered, if a person falls down on the floor and remains motionless.*

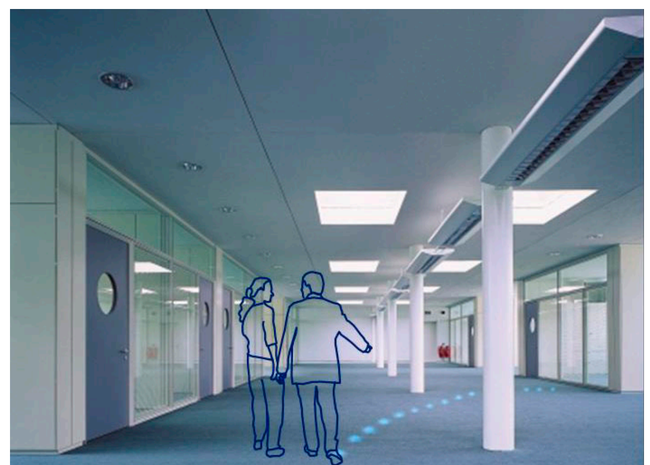


Figure 5: *LEDs showing the next emergency exit in case of i.e. a fire alarm.*

UPnP Compliant System Architecture for Embedded Transceivers in Low Power Sensor Networks

Introduction

In the future, the networking and interoperation of manifold appliances will play an increasingly important role, fostering the vision of ambient intelligence environments to be put into reality. Most often, home automation systems are considered, but also health care applications, information spreading beacons as well as maintenance and control of white goods are in the scope of ambient intelligence scenarios.
For all these applications, networked wireless sensors and actuators are essential components. They provide certain information or execute controlled actions. To ensure user acceptance, these components must be cheap and energy-efficient. Moreover, wireless control networks in smart environments must be able to organize themselves dynamically and autonomously.
To this end, semantic middleware platforms provide mechanisms which allow the nodes to discover each other, to offer their functionality to other nodes in a formalized way as so-called services, and to access remote services offered by other nodes. Currently, one of the best promoted middleware standards is Universal Plug and Play™ (UPnP). Due to semantic control facilities, UPnP's protocols are complex and require more computing power and memory than usually available in small embedded sensor and actuator devices.
Therefore, we have developed a novel system architecture called Sindrion. It relies on sourcing out complex data processing from the sensor nodes to dedicated terminals which establish a proxy in the UPnP network. As we will show subsequently, this allows flexible, highly-functional, UPnP compliant devices while concurrently satisfying rigid cost and power requirements.

Basic principle

The basis of the Sindrion system is to set up a wireless link between peripheral devices and computing terminals to source out complex data processing from the peripherals to the terminals [150]. A peripheral device contains a small smart transceiver, the so-called Sindrion Transceiver, which is attached to embedded sensors or actuators (see Fig. 6). Typical peripheral devices are environmental sensors, small actuators like switches, or home appliances. They bear very limited or no computing power, and the embedded sensors and actuators can be controlled by simple proprietary analog or digital control lines. These are connected to the input- and output ports (I/O ports) of the Sindrion Transceivers.
The terminal is equipped with an RF transceiver which is compatible with that included in the Sindrion Transceiver. Data and protocol processing are done in the terminal, which features a virtually unlimited amount of processing power and memory compared to the Sindrion Transceiver.

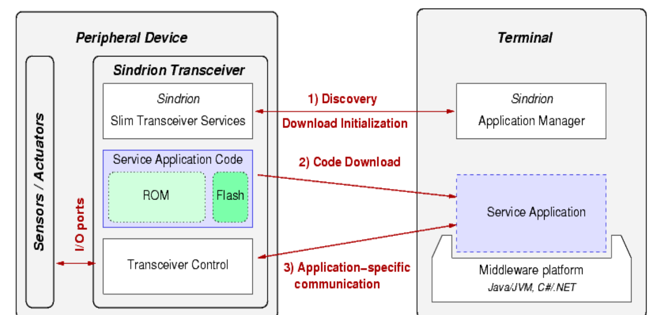


Figure 6: *Sindrion system architecture.*

Fig. 6 shows the fundamental sequence of establishing the communication between the terminal and a previously unknown Sindrion Transceiver. The procedure is as follows:

1) **Discovery**: The two end devices find each other in the discovery phase using the UPnP discovery protocol.
2) **Code Download**: If the terminal does not yet contain the control application for the Sindrion Transceiver, the transceiver's platform-independent Java application code is downloaded and then executed on the terminal. High-level programming languages facilitate application development.
3) **Application-Specific Communication**: The following communication between the downloaded service application on the terminal and its counterpart, the transceiver control protocol on the Sindrion Transceiver, is completely unsemantic and does not have to be defined by any standard.

The Sindrion Sensor Node as UPnP Device

The Universal Plug and Play (UPnP) Architecture is one of the best established middleware platforms for Ubiquitous Computing. UPnP uses open and standardized protocols on top of the common TCP/IP or UDP/IP stack (see Fig. 7). They are based on XML and allow to describe and control devices in a formalized way. The most important advantages of UPnP are the semantic interoperability of devices from different vendors and the simple extensibility to future devices.
However, there is a high demand for memory and computing power for UPnP Devices since variable XML-based messages have to be processed.

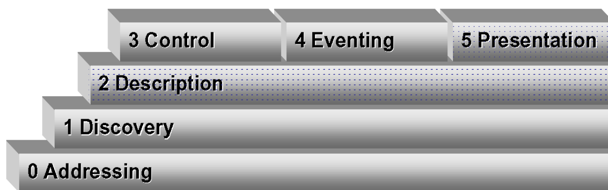


Figure 7: *UPnP Device Architecture.*

The complexity of UPnP control and eventing prevents a cheap and low-power device to implement the complete UPnP Device Architecture.
Thus, every Sindrion Transceiver acts as so-called UPnP Basic Device, which is a special device type without embedded UPnP services (see the shaded area in Fig. 7). The Basic Device supports the UPnP discovery, and description mechanisms as well as the so-called presentation layer, which quasi implements web server functionality. These require much less computational effort than UPnP control and eventing.
According to the Sindrion system architecture, there are two ways to integrate the transceivers into the UPnP environment [155]:

1. **UPnP Basic Device:**
   A Java applet is downloaded from the transceiver to the terminal. It is executed in a Web browser environment to control the transceiver.

2. **Complete UPnP Device:**
   For extended control, the downloaded service application consists of a UPnP device proxy which provides service control and eventing. The device proxy is maintained by the Sindrion Application Manager (AM) on the terminal, which handles the proxies' life-cycle and provides hand-over functionality (see Fig. 8). A code repository caches the service applications and also distributes them to other Application Managers in the network. The UPnP Proxy translates the unsemantic communication protocol into full-fledged XML-based UPnP control and eventing messages.

To extend the scope of usage to OSGi components, the standardized OSGi/UPnP mapping can be used in the service applications.

Figure 8: *Sindrion Transceivers as part of a UPnP Distributed System.*

With the given software architecture, a Sindrion Transceiver is seamlessly embedded into the UPnP environment. The underlying scheme is transparent to the other members of the UPnP network - the sensor node just appears as a fully enabled UPnP Device as shown in Fig. 8.
Thus, different network nodes can interact by the UPnP interface to form complex services. For example, a thermometer device may provide temperature data to a small LCD display in another room, at the same time to a PC to store a temperature timeline, and to an HVAC system for ventilation control.
In order to show feasibility and applicability of the Sindrion system architecture, we realize a transceiver module as a prototype system. The focus of the implementation lies on the joint optimization of the hardware architecture and network protocols to come to a cost and power optimized system solution.

Guido Stromberg
Phone +49 (0)89 234-40430
E-Mail guido.stromberg@infineon.com

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Contact:
Infineon Corporate Research
Phone: +49 (0)89 234-46900
E-mail: corporate_research@infineon.com

Published by Infineon Technologies AG