

## LNQE-Kolloquium 02.12.2014

Das Laboratorium für Nano- und Quantenengineering und IEEE CAS Germany Section Chapter laden im Rahmen des IEEE Distinguished Lecturer Program (DLP) ein:

Dienstag, 02.12.2014 um 17:30 Uhr + anschließendes Get-Together  
im Seminarraum + Foyer des LNQE-Forschungsbaus (Gebäude 3430),  
Schneiderberg 39, 30167 Hannover, Deutschland

# „Technology and Circuit Co-design for overcoming Low Power Barriers in nm era“

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Low Power is a universal theme which is pushing system software and hardware. In order to achieve low power system, circuit and technology co-design is essential. This talk focuses on related technology and important circuit techniques for nanoscale era. Achieving low power and high performance simultaneously is always difficult. Technology has seen major shifts from bulk to SOI and then to non-planar devices such as FinFET/Trigates.

This talk consists of pros and cons analysis on technology from power perspective and various techniques to exploit lower power. As the technology pushes towards sub-65nm era, process variability and geometric variation in devices can cause variation in power. The reliability also plays an important role in the power-performance envelope. This talk also reviews the methodology to capture such effects and describes all the power components. All the key areas of low power optimization such as reduction in active power, leakage power, short circuit power and collision power are covered. Usage of clock gating, power gating, longer channel, multi-Vt design, stacking, header-footer device techniques and other methods are described for logic and memory. Finally the talk summarizes key challenges in achieving low power.

Dr. Rajiv V. Joshi is a research staff member at T. J. Watson research center, IBM. He received his B.Tech I.I.T (Bombay, India), M.S (M.I.T) and Dr. Eng. Sc. (Columbia University). His novel interconnects processes and structures for aluminum, tungsten and copper technologies which are widely used in IBM for various technologies from sub-0.5 $\mu\text{m}$  to 14nm. He has led successfully pervasive statistical methodology for yield prediction and also the technology-driven SRAM at IBM Server Group. He commercialized these techniques. He received 3 Outstanding Technical Achievement (OTAs), 3 highest Corporate Patent Portfolio awards for licensing contributions, holds 54 invention plateaus and has over 200 US patents and over 350 including international patents. He has authored and co-authored over 175 papers. He is inducted into New Jersey Inventor Hall of Fame in Aug 2014 along with pioneer Nicola Tesla (<http://www.njinvent.org/awards/Awards2014.html>). He is a recipient of 2013 IEEE CAS Industrial Pioneer award and 2013 Mehboob Khan Award from Semiconductor Research Corporation. He is a member of IBM Academy of technology and master inventor. He is Distinguished Lecturer for IEEE CAS and EDS society. He is IEEE and ISQED fellow and distinguished alumnus of IIT Bombay. He serves as an Associate Editor of TVLSI. He served on committees of ISLPED (Int. Symposium Low Power Electronic Design), IEEE VLSI design, IEEE CICC, IEEE Int. SOI conference, ISQED and Advanced Metallization Program committees. He served as a general chair for IEEE ISLPED. He is an industry liaison for universities as a part of the Semiconductor Research Corporation. Also he is in the industry liaison committee for IEEE CAS society.

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